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# ASML

#### Integration of a Fab Cyber Physical System The marriage of two digital twins

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ASML, System Engineering

SASG, Eindhoven June 4th, 2019 v1

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Slide 2

Summary

**Topics** 

ASML is a patterning/lithography company Chips are made with data

Two digital twins are horizontally and vertically integrated

Horizontal integration is the most challenging

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Slide 3

Summary

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# It's hard to imagine a world without chips



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### Example: Self-driving truck (expected between next year and 2025)





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#### Founded in 1984 as a spin-off from Philips



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### A global presence with >23,000 employees



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# Our key locations



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#### All major chipmakers are our customers

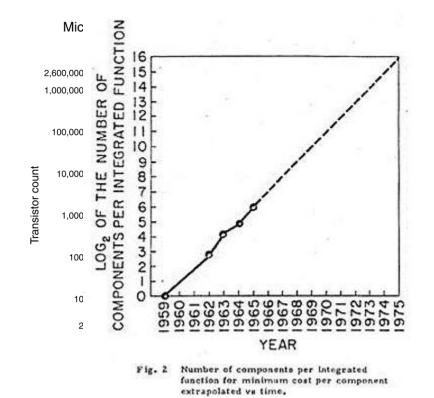
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Company	Segment	2018 capex (est., \$B)
SAMSUNG	Foundry + Memory	24.0
intel	Integrated Devices	14.0
tsinc	Foundry	11.0
SK hynix	Memory	11.0
Micron	Memory	8.5
TOSHIBA <i>ivid</i> Western Digital'	Memory	7.3
	Foundry	4.5
SMIÇ	Foundry	1.9
UMC	Foundry	1.1
SONY	Others	1.0
Others		30.7
Total		115.0

#### Driving the semiconductor industry: Moore's Law



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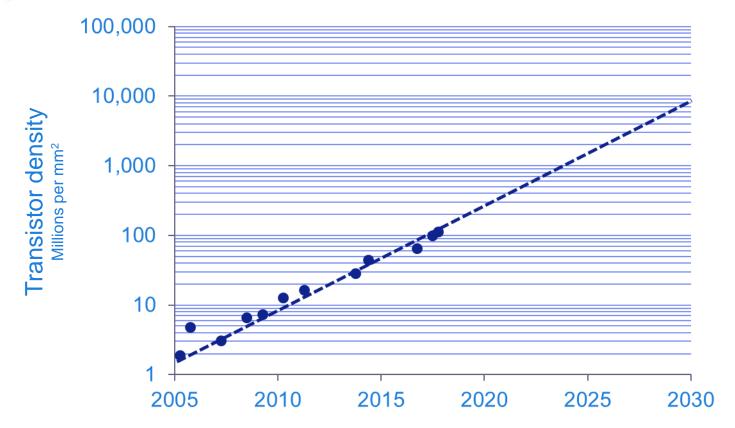
Gordon Moore (1965): Number of transistors per chip doubles every year.

Later adjusted to two years, the trend has held for more than four decades.

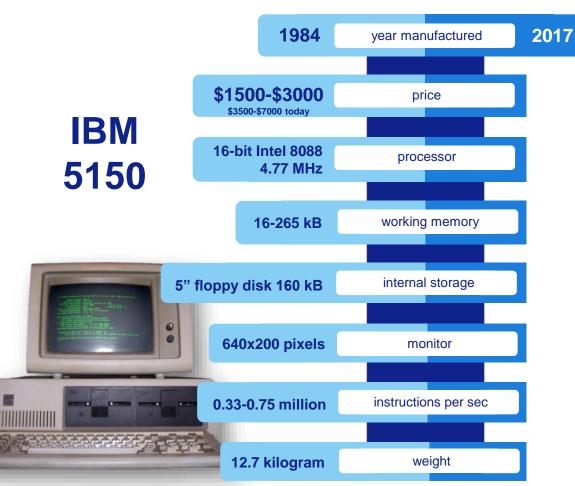
#### We see this trend continuing beyond the next decade Our industry is moving towards 1 billion transistors per mm<sup>2</sup>

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#### Moore's Law powers innovation and lowers cost



Apple iPhone X

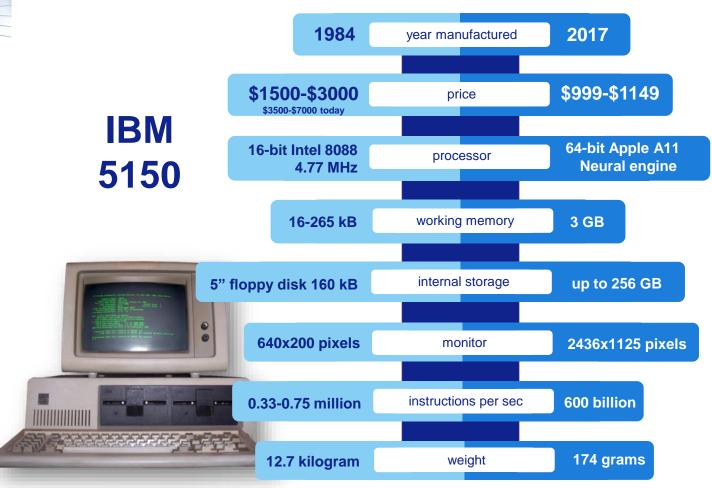
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Q3 2018



### Moore's Law powers innovation and lowers cost



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Apple iPhone X



### Keeping up with Moore's Law

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**1984** PAS 2000 ASML's first stepper

#### 2015 TWINSCAN NXT:1980Di Our most advanced

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immersion system

2018 TWINSCAN NXE:3400B High volume EUV system

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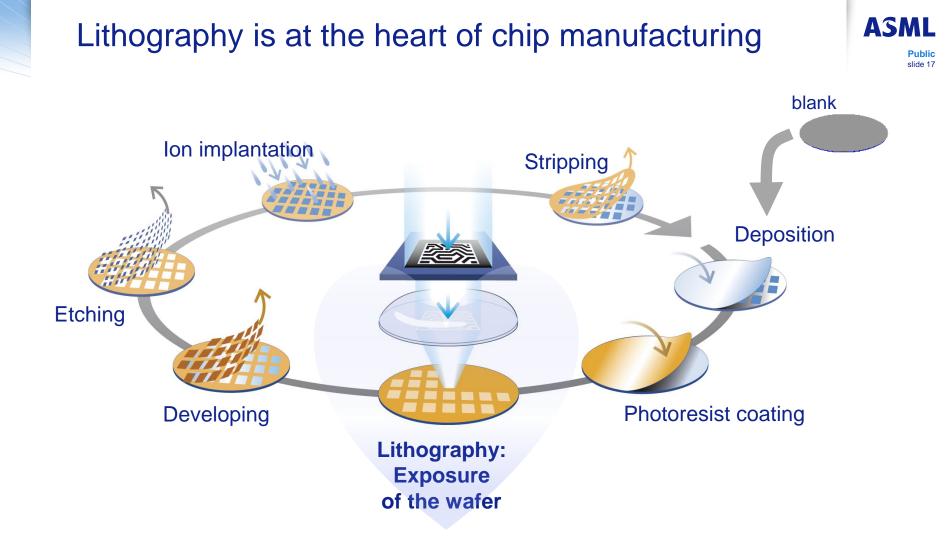
#### Summary

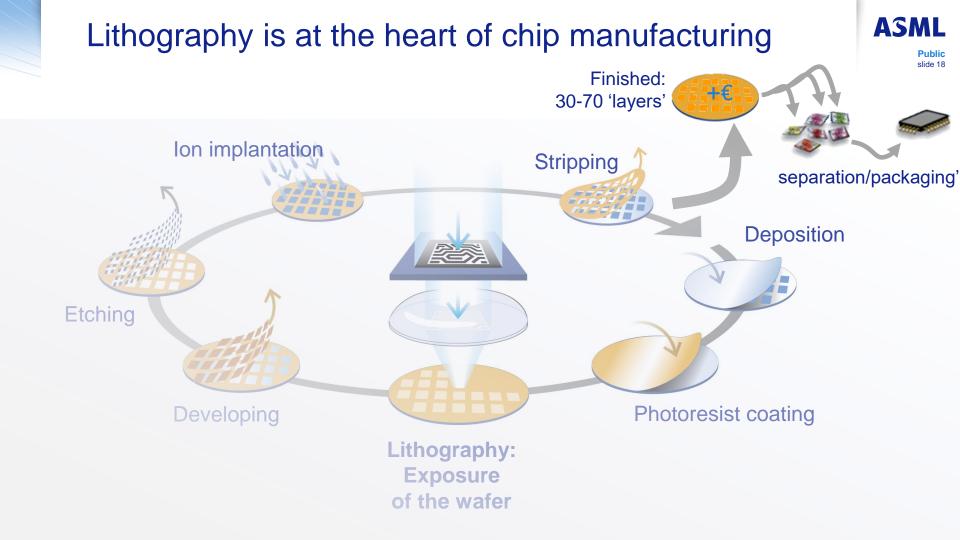
## ASML is a patterning/lithography company

Chips are made with data

Two digital twins are horizontally and vertically integrated

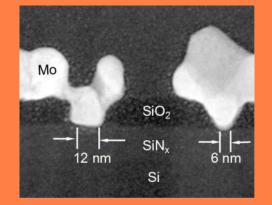
Horizontal integration is the most challenging





# Keeping up with Moore's Law

# Structure in a chip: 6 nanometer detail





#### **1984** PAS 2000 ASML's first stepper

#### 2015 TWINSCAN NXT:1980Di Our most advanced immersion system

2018 TWINSCAN NXE:3400B High volume EUV system

## Keeping up with Moore's Law

Wavelength: 13.5 nanometers

Resolution: ≤ 22 nanometers

Overlay: 1.0 nanometers

> Wafer size: 300 mm

Productivity: 125 wafers per hour

**1984** PAS 2000 \SML's first steppe

#### 2015 TWINSCAN NXT:1980Di Our most advanced immersion system

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2018 TWINSCAN NXE:3400B High volume EUV system Public Slide 20 Q3 2018

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# Control at nm level is really fine-grained

1 mm motion on scale of The Netherlands (300 km Ø)

1:300,000,000



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# Control at nm level is really fine-grained

1 mm motion on scale of The Netherlands (300 km  $\emptyset$ )

1:300,000,000

1 nm motion on scale of wafer (300 mm Ø)

1:300,000,000

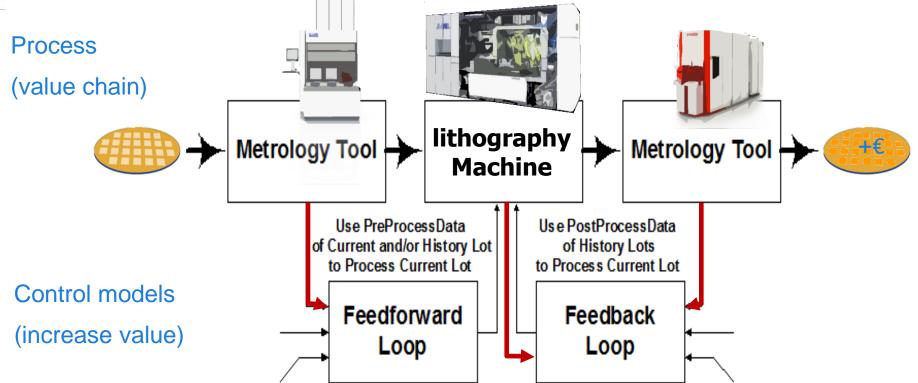


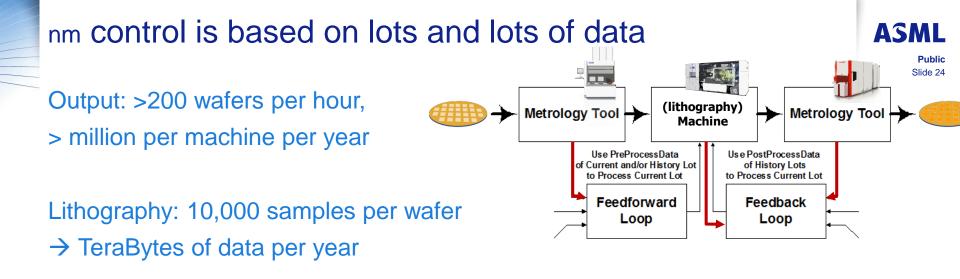
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# nm control is about integration of metrology (measuring)

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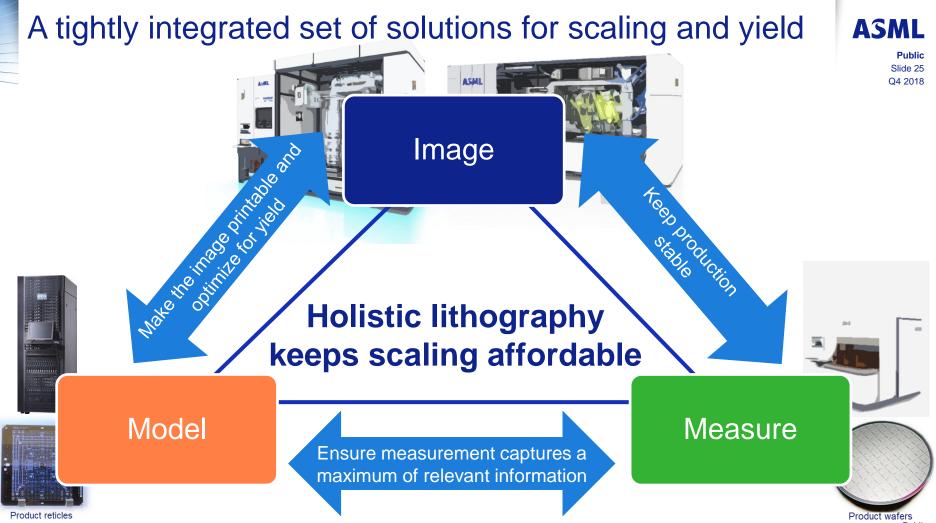
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Metrology tool: 100-10,000 samples per wafer → TeraBytes of data per year

Fabs use this to control every square  $mm^2$  of every wafer: Input per wafer: 100,000 x 6 axis = 600,000 inputs/wfr



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#### Summary

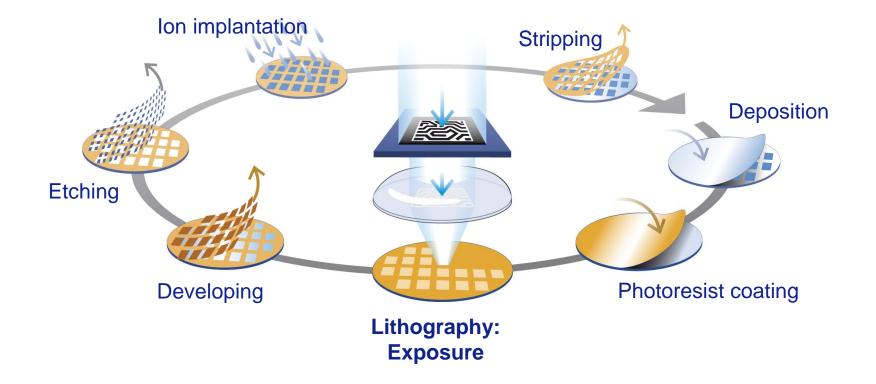
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### Lithography value chain: 700+ steps

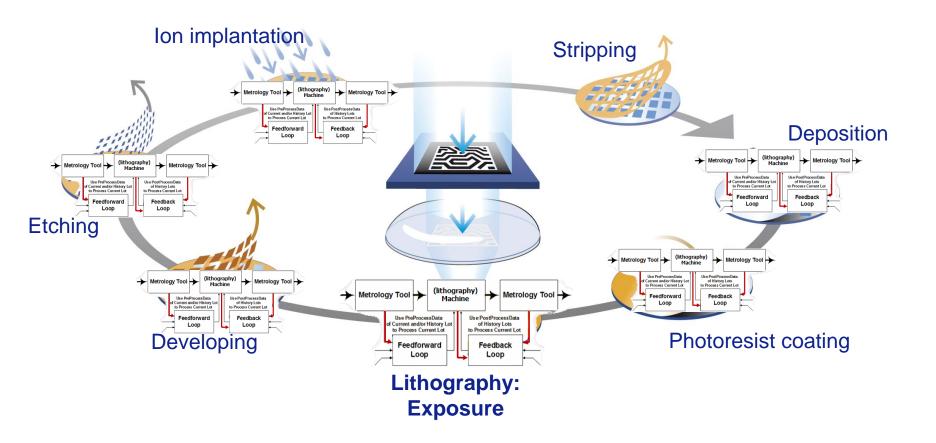


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# Lithography is horizontally integrated in 700+ steps



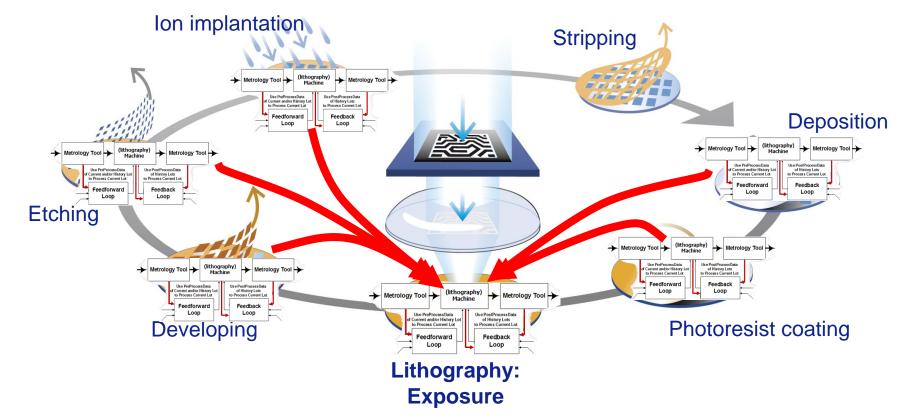


#### Lithography is horizontally integrated in 700+ steps Upstream and down stream steps feed data into our litho models

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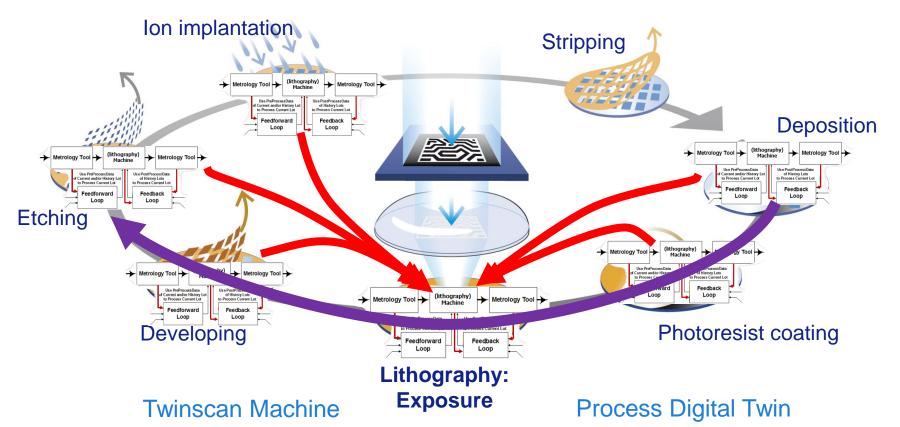
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Lithography is horizontally integrated in 700+ steps Upstream and down stream steps feed data into our litho models so the patterns 'after etch' come out almost nm-perfect. ASML

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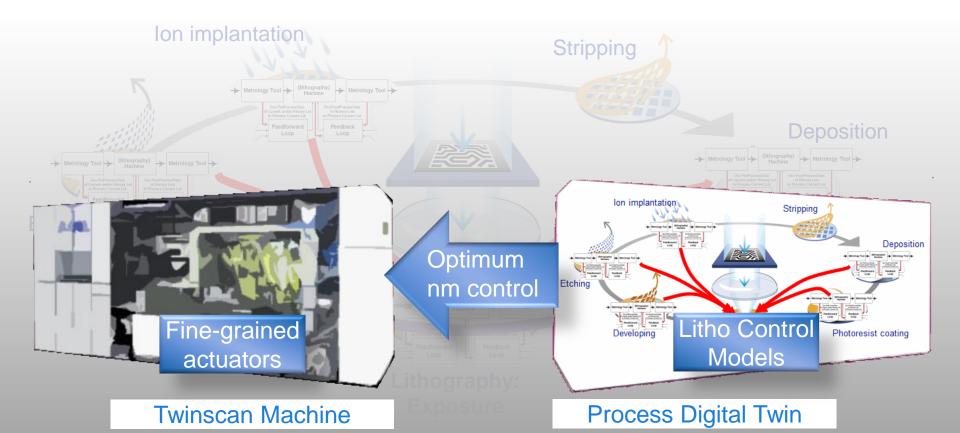


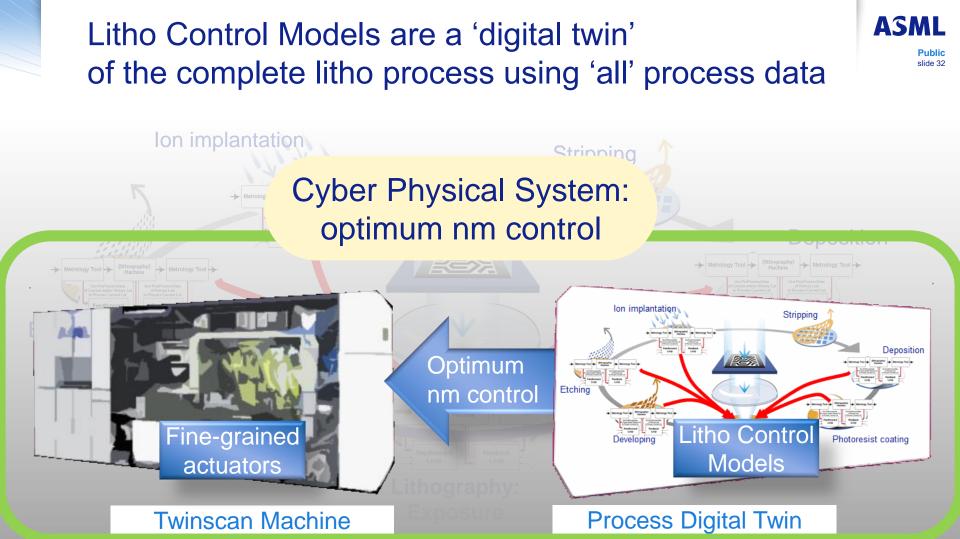
# Litho Control Models are a 'digitital twin' of the complete litho process using 'all' process data

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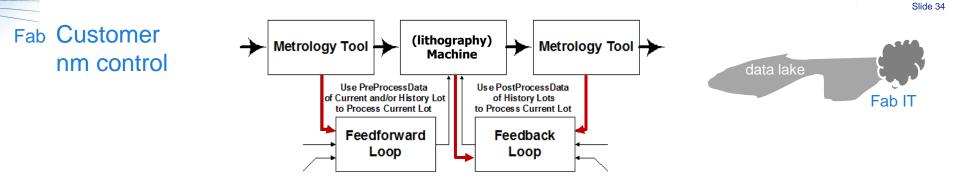
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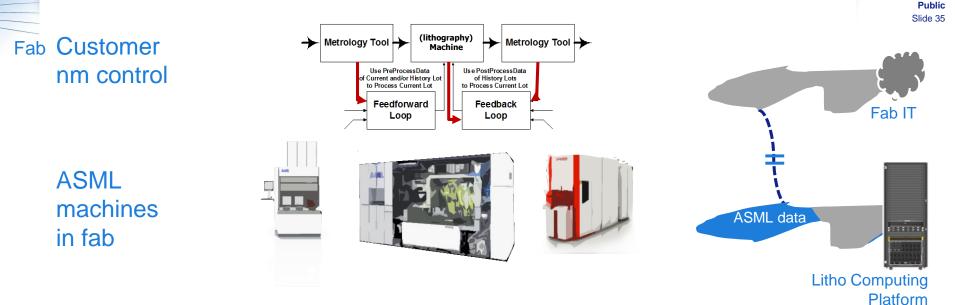
#### Vertical 'integration': separate data lakes fab/ASML



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## Vertical 'integration': separate data lakes fab/ASML



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## Vertical 'integration': separate data lakes fab/ASML

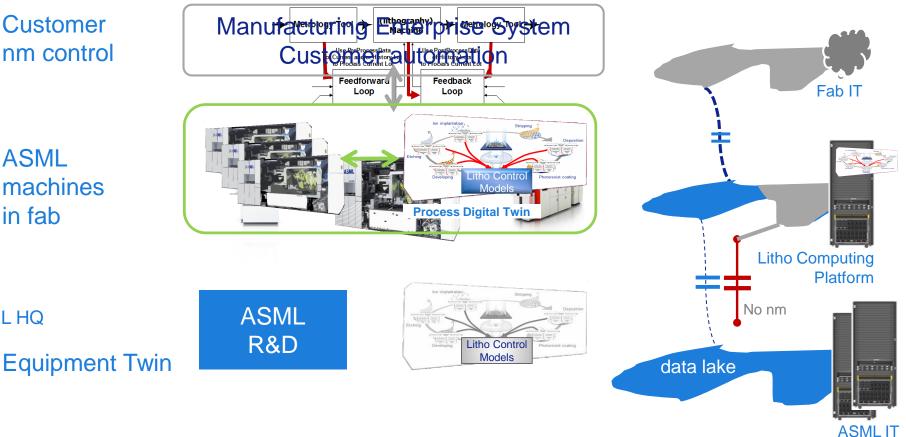
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ASML HQ

Fab Customer



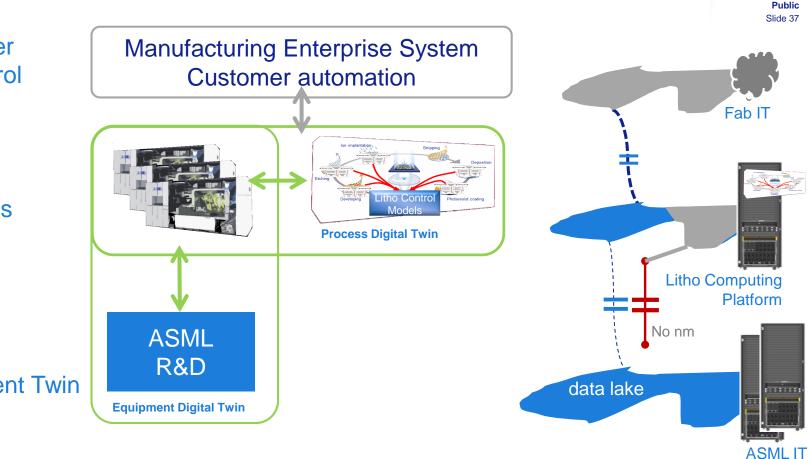
# Two digital twins, not yet happily married

Fab Customer nm control

> ASML machines in fab

ASML HQ

Equipment Twin



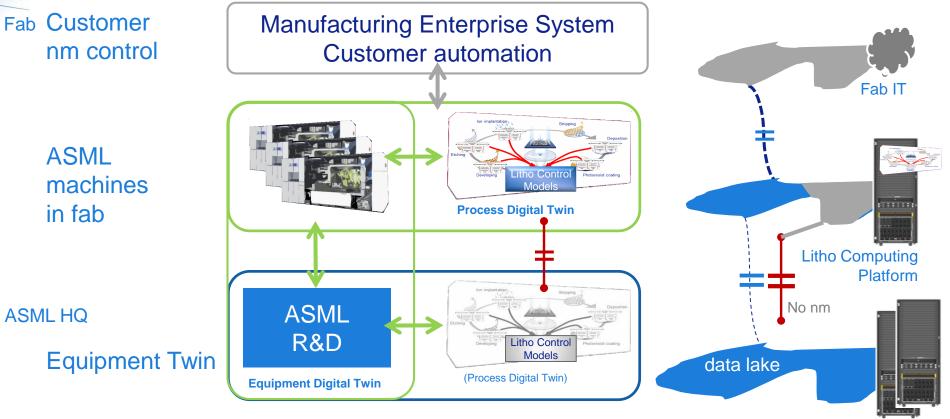
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# Two digital twins, happily married

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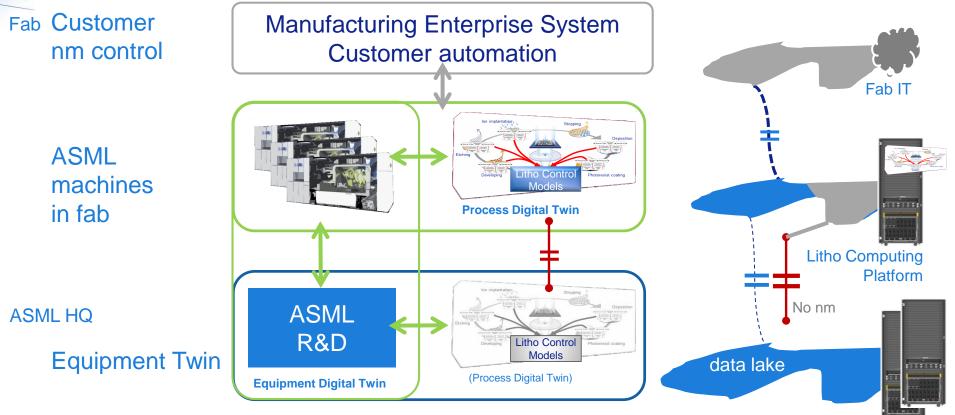
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## Vertical integration is challenging but doable

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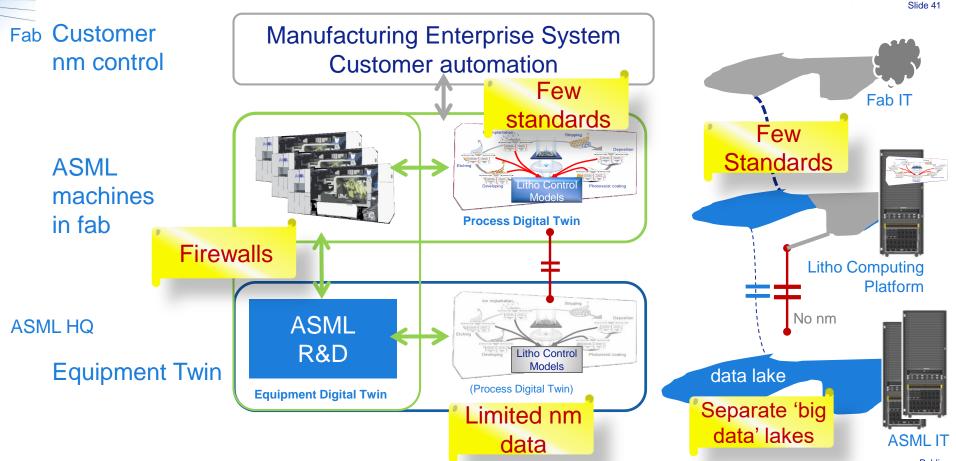
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#### Vertical integration is challenging but doable



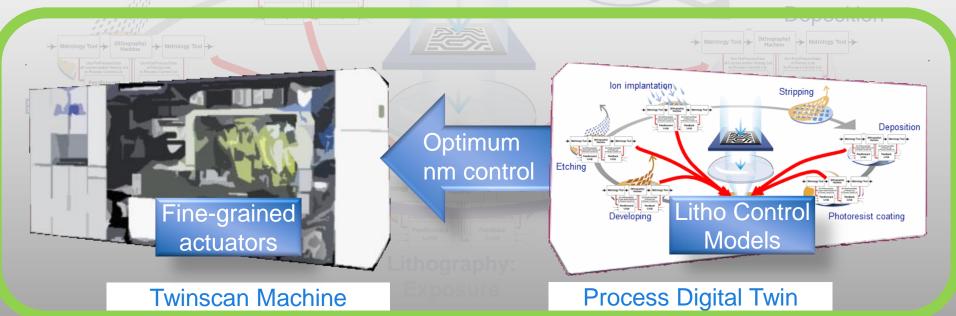
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#### Horizontal integration is the most challenging

- This is our customers' expertise and value chain  $\rightarrow$  team up
- ASML does not (can not) get all nm data  $\rightarrow$  link data lakes
- nm control implies ppb (part per billion) accuracy levels: subtle trends, 1:1,000,000 incidents → access to 'all' data needed



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Horizontal and vertical integration happens, driven by economics (i.e. nm gain)

Standards for vertical integration are essential to allow cross-enterprise cooperation to work

Horizontal integration – via teams – requires a way to have interoperable CPS'es and Data Lakes

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#### Recap

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