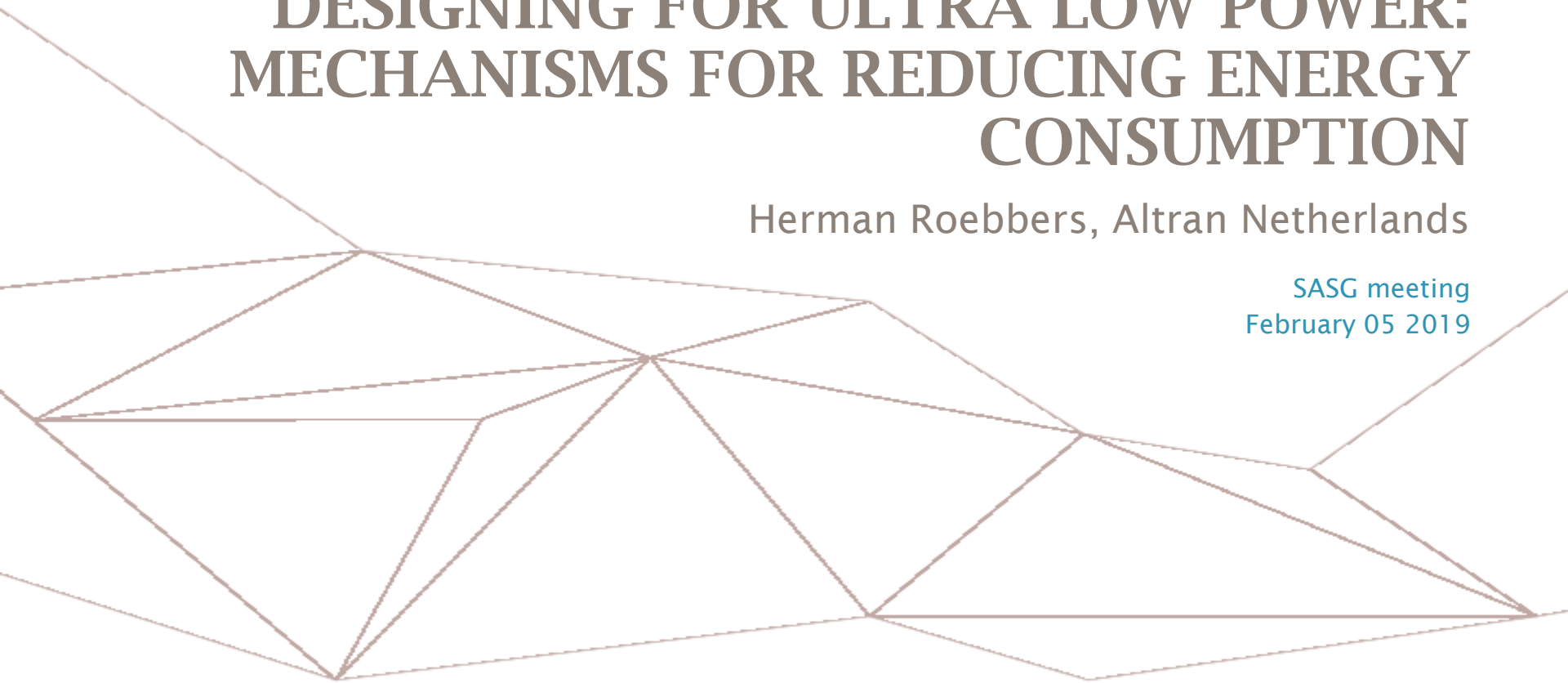
DESIGNING FOR ULTRA LOW POWER: MECHANISMS FOR REDUCING ENERGY CONSUMPTION

Herman Roebbers, Altran Netherlands

SASG meeting
February 05 2019



MAKING INNOVATIONS MATTER

altran

I HAVE A DREAM

IoT Edge Node

Energy Harvester

IoT Edge Node

WHY LOSE THE BATTERIES?

Think 20 bln IoT devices

- That's **tens of billions** of spent batteries/yr!
- A huge environmental burden
  - Toxic
  - Explosive
- Huge cost of batteries and replacement
  - Replacement not always possible
    - Sensor poured in concrete

GOAL

Energywise self-sustaining Sensor nodes

- ULP is a necessity for IoT wireless end nodes
- Requires system thinking
- How so?

INTRODUCTION

Herman Roebbers, Expert @ Altran

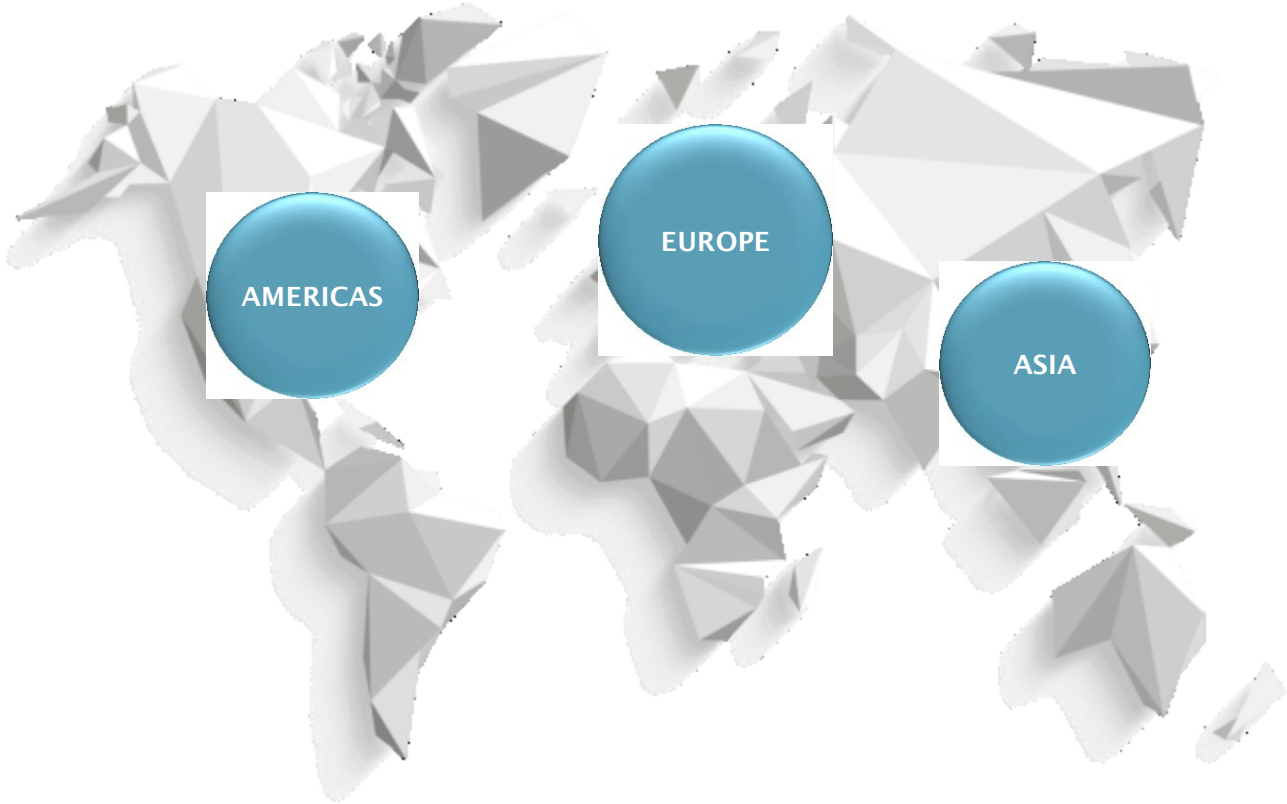
ALTRAN: GLOBAL LEADER
IN ENGINEERING AND R&D SERVICES

20+
Countries

28.000+
Innovation Makers

9
Industry segments

€ 1.945
2015 Revenues



INTRODUCTION

Herman Roebbers, Expert @ Altran NL

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INTRODUCTION

Who did I work with or for

Figure 1. PCB of the micro-SDIO base station

INTRODUCTION

ULP related activities

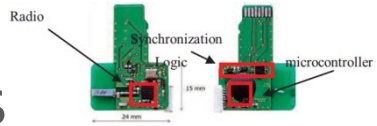

Figure 1. PCB of the micro-SDIO base station

Holst Centre, 2009 – 2011: in ULP group, working on code and architecture of WBAN radio and base station (HW and SW). Co-authored conference paper on interfacing WBAN base station to Android mobile phone. Benchmarking Holst Centre ASIC against EFM32 Gecko for ECG data processing.

Holst Centre
Open Innovation by imec and TNO

EEMBC, 2016 –:external advisor to 3 Working Groups:
ULPMark (CoreProfile and Peripheral Profile)
IoTMark-BLE
SecureMark

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Windesheim

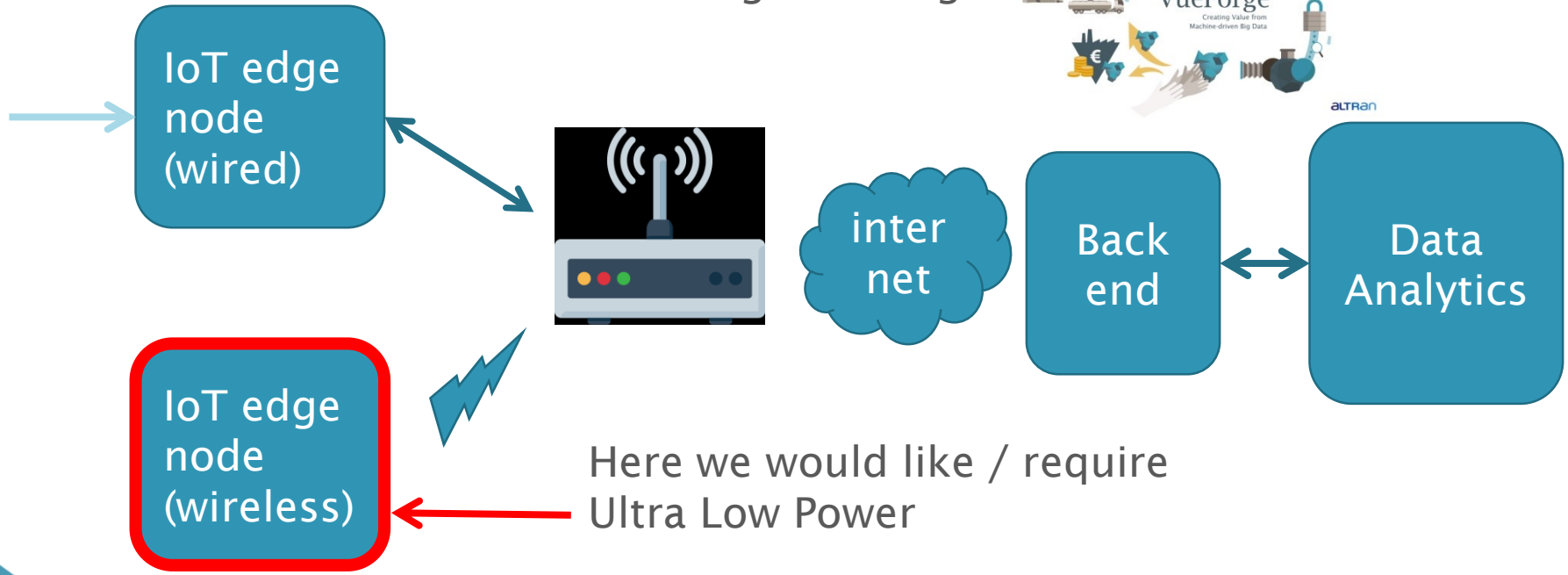
NWO Toegepaste en Technische Wetenschappen

ZERO: Towards Energy Autonomous Systems for IoT

INTERNET OF THINGS

High level diagram

e.g. VueForge

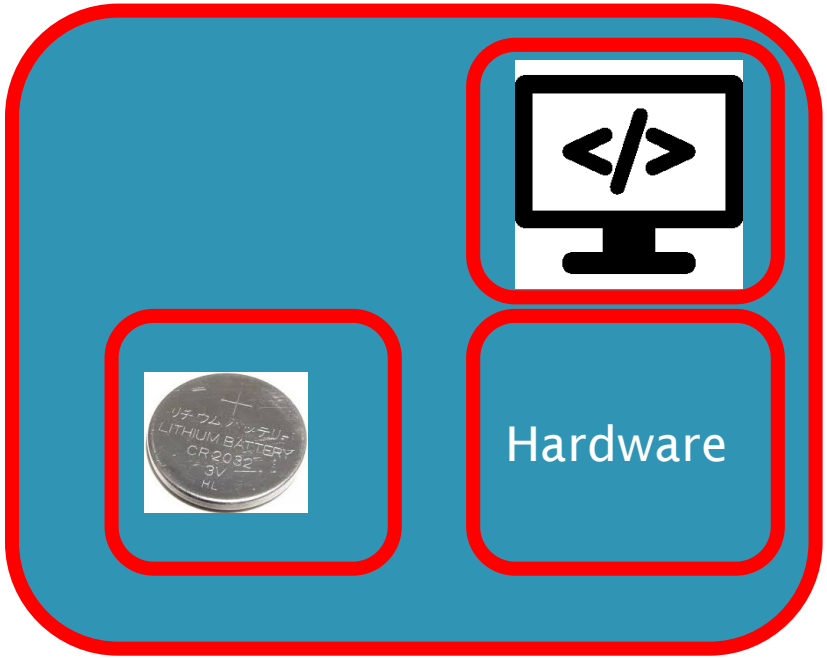


ANATOMY OF AN IOT EDGE NODE

- Where we (mostly) are

IoT edge node (wireless)

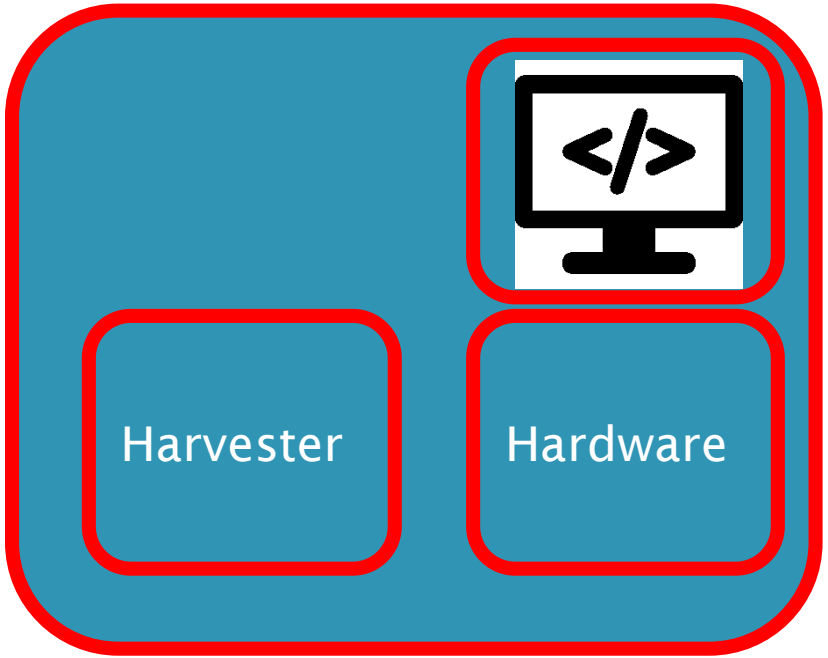
=



ANATOMY OF AN IOT EDGE NODE

- Where we need to be

IoT edge node (wireless)



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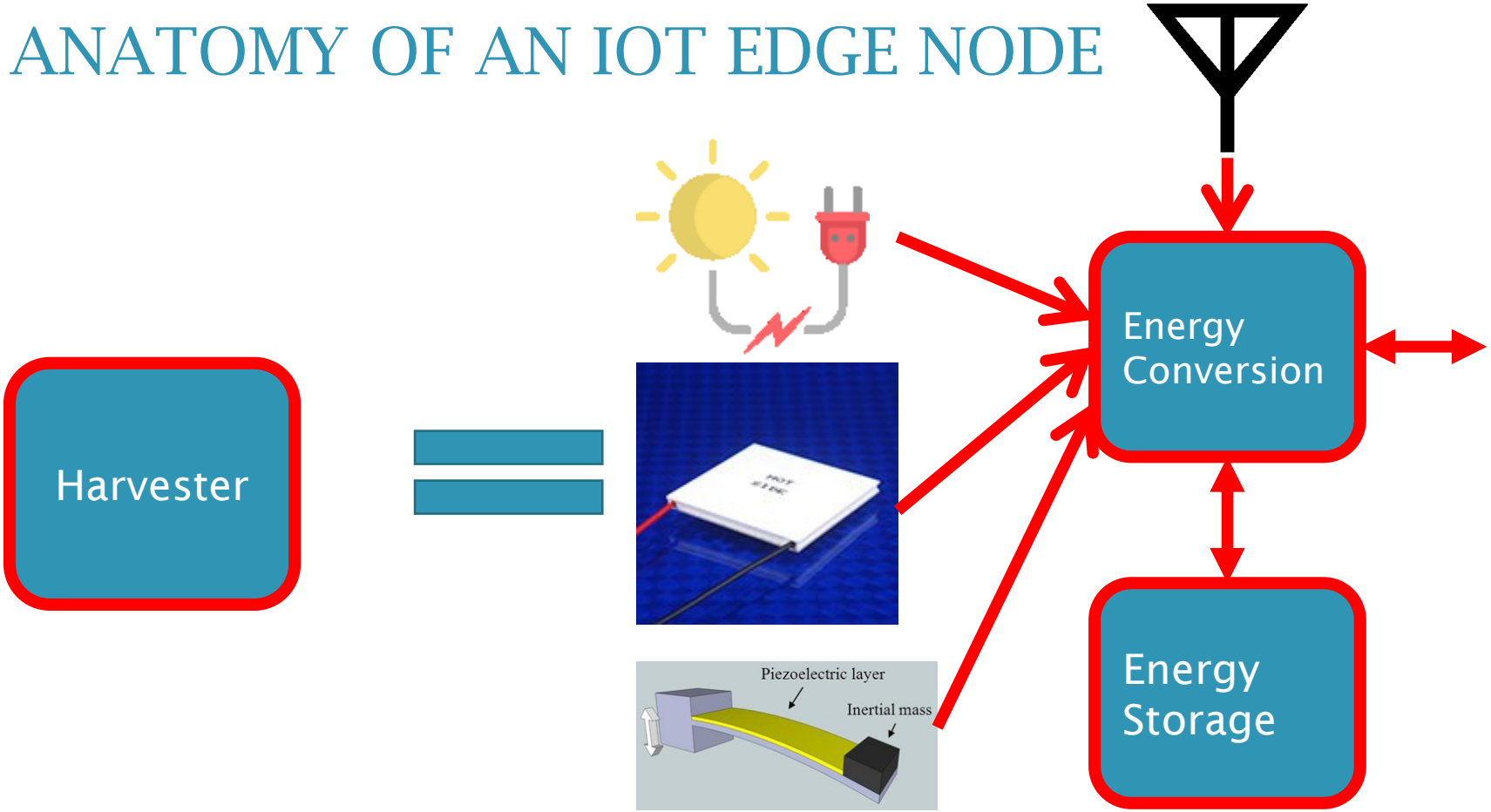


http://www.npl.co.uk/upload/img/piezoelectric-energy-harvester.jpg

HOW DO WE GET THERE

- Minimize energy consumption
- Harvest the necessary energy

How good can we get (Quality of Results)?

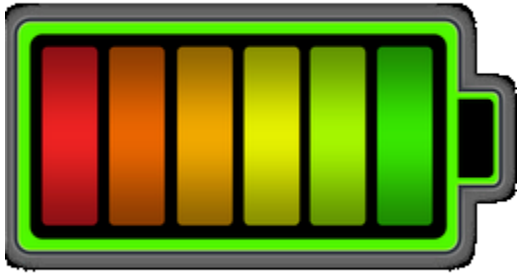
- HW often chosen for you (COTS)
  - "Second best" : make do with available HW
  - But at least understand what you have
- You could do better if you also design the HW
  - Much bigger job, might be the only way

HOW TO MINIMIZE ENERGY CONSUMPTION

Define a process for achieving it

- How energy efficient is my system?
  - Run EEMBC benchmarks to create baseline measurements
  - Measure energy consumption of operation scenarios (in CI/CD setup)
- Key MCU characteristics for ULP
- What “knobs” to turn?

WHY ULTRA LOW POWER?



- Long operating lifetime required
- Changing batteries is expensive/impossible
- Employing people to do it is even more expensive
- Batteries are environmental hazard
- Because regulations require it

- Even when powered by mains, reduction of energy consumption diminishes pollution by power plants

When using really little power: Harvest energy from environment (solar/thermo/piezo/vibration/…)

ANATOMY OF AN IOT EDGE NODE

Hardware

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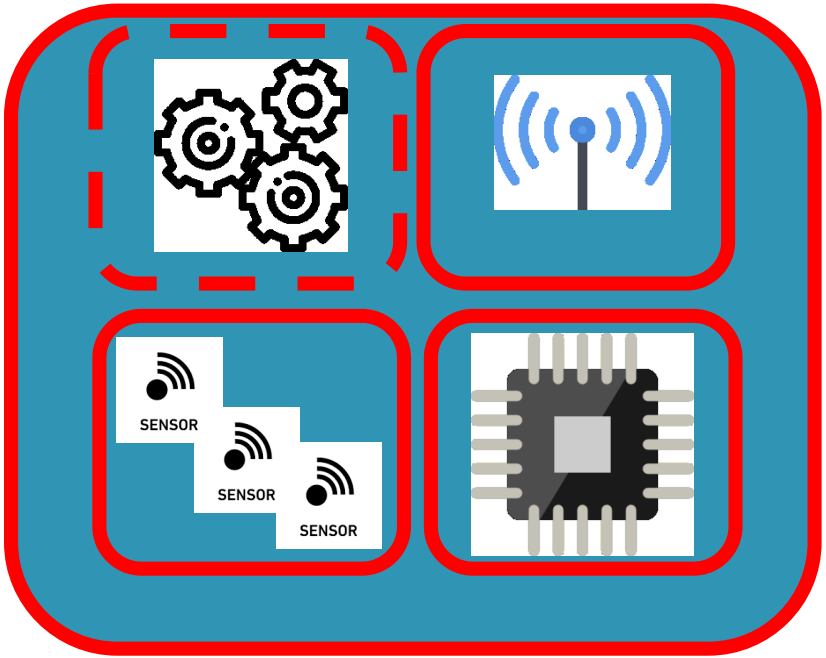
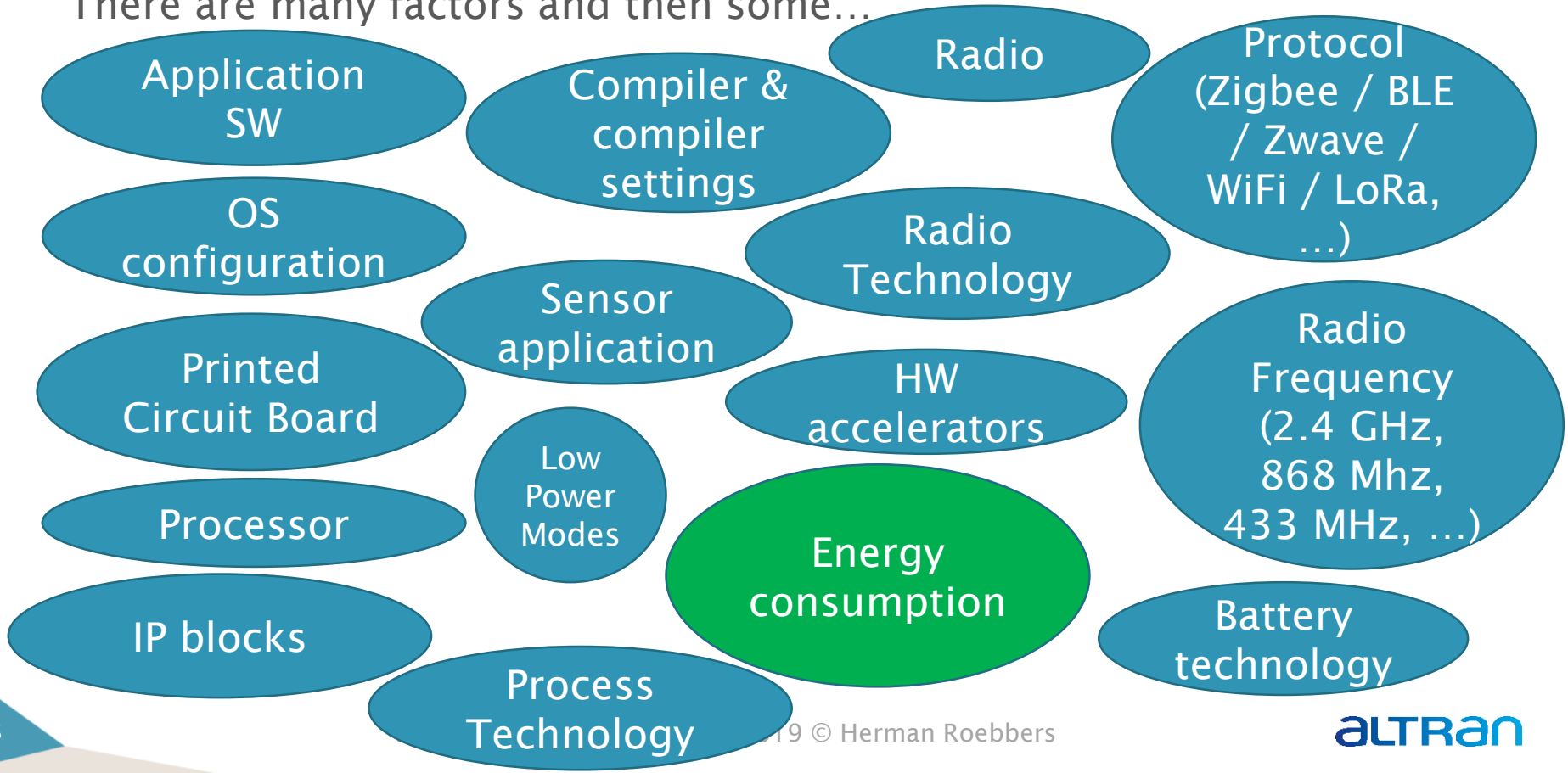


FACTORS INFLUENCING ENERGY CONSUMPTION

There are many factors and then some…



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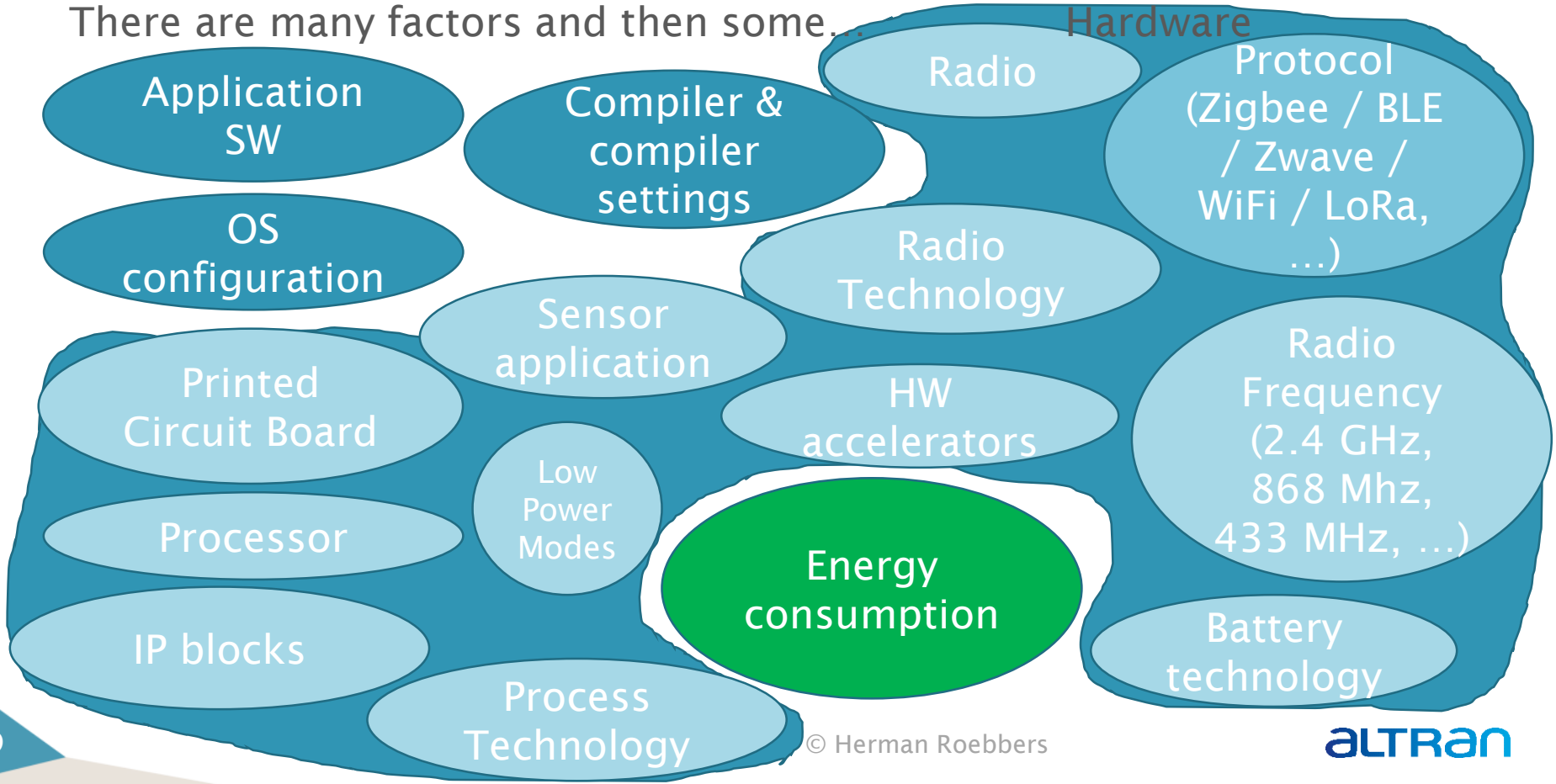

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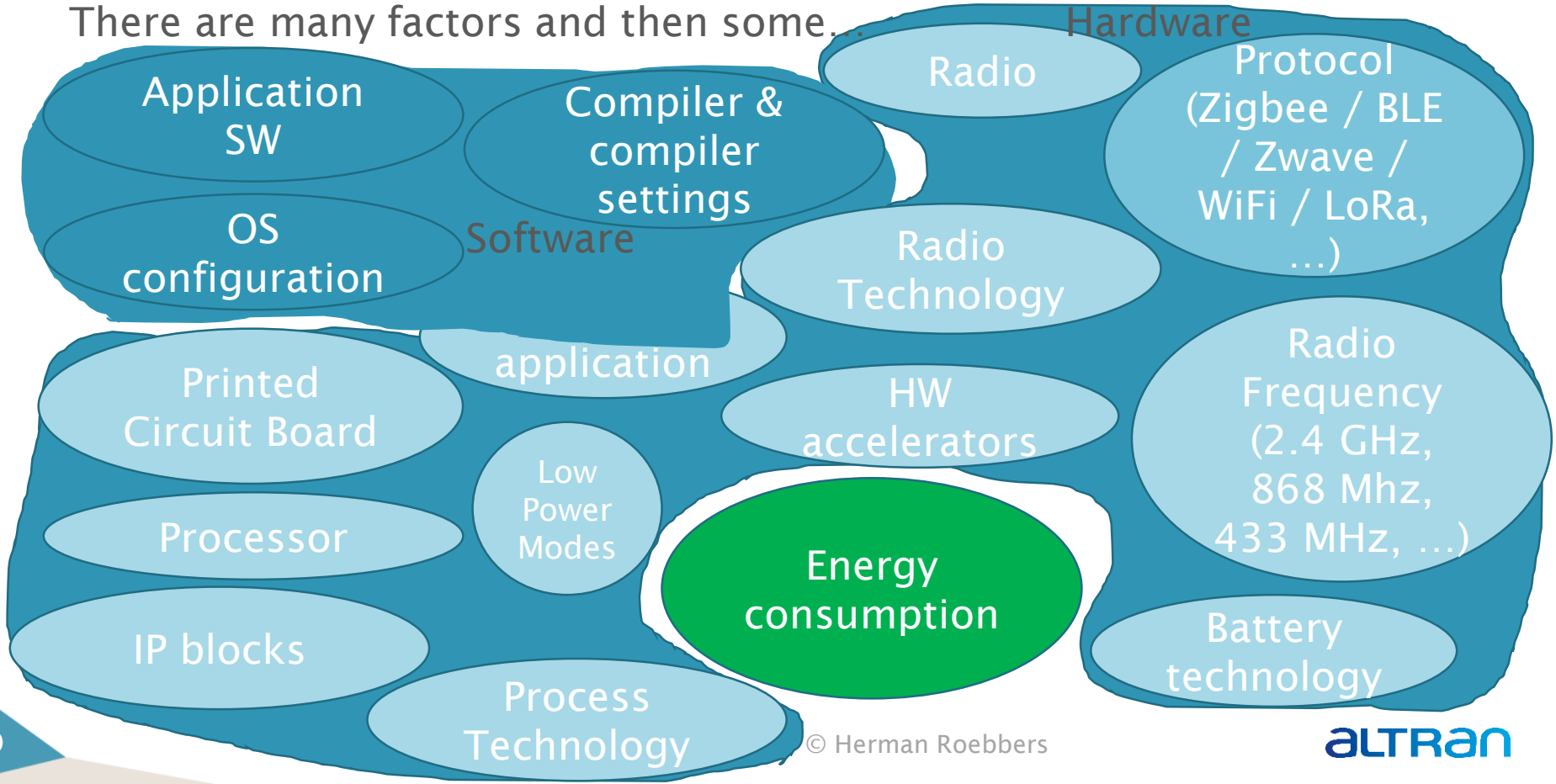

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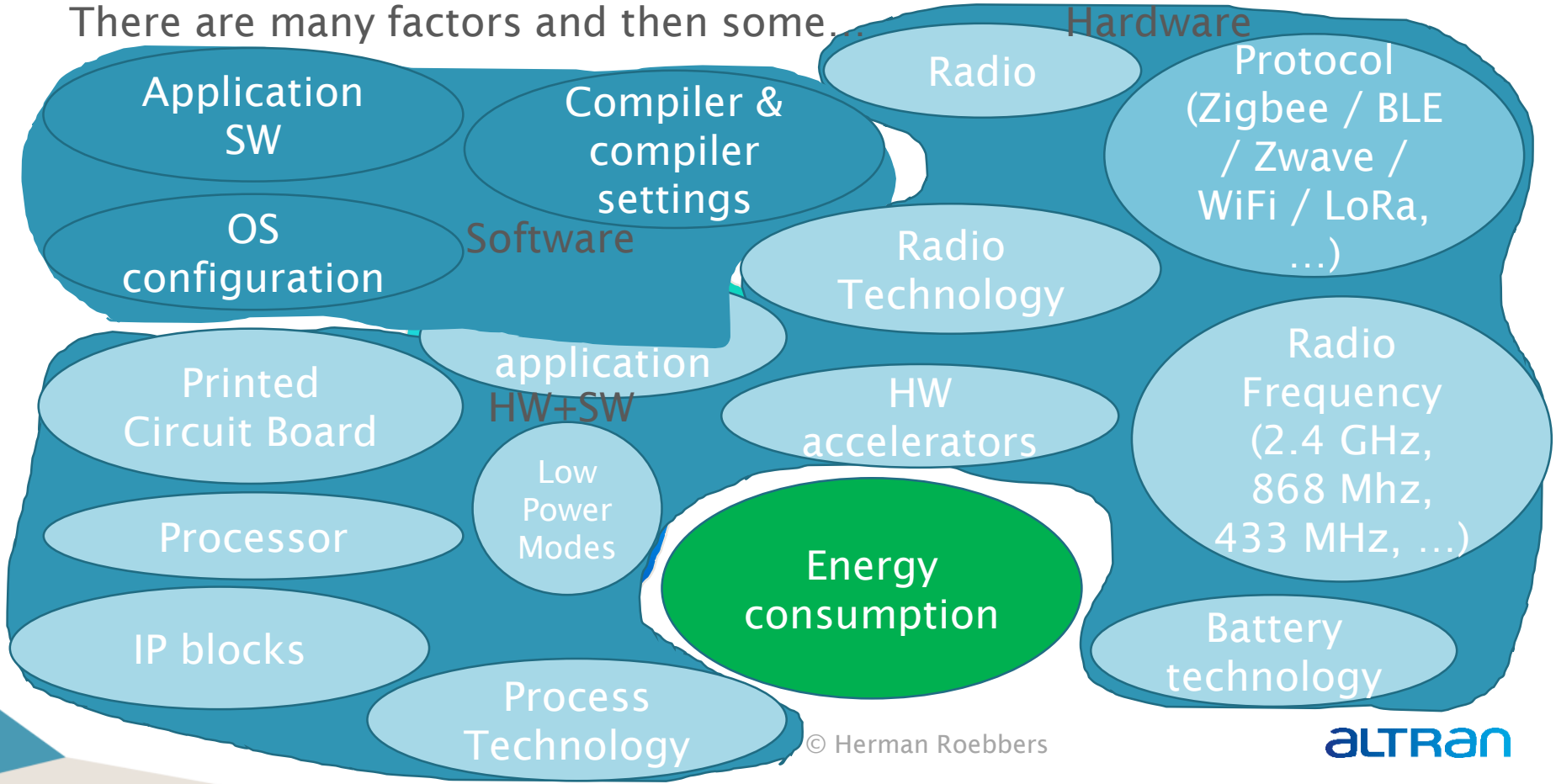

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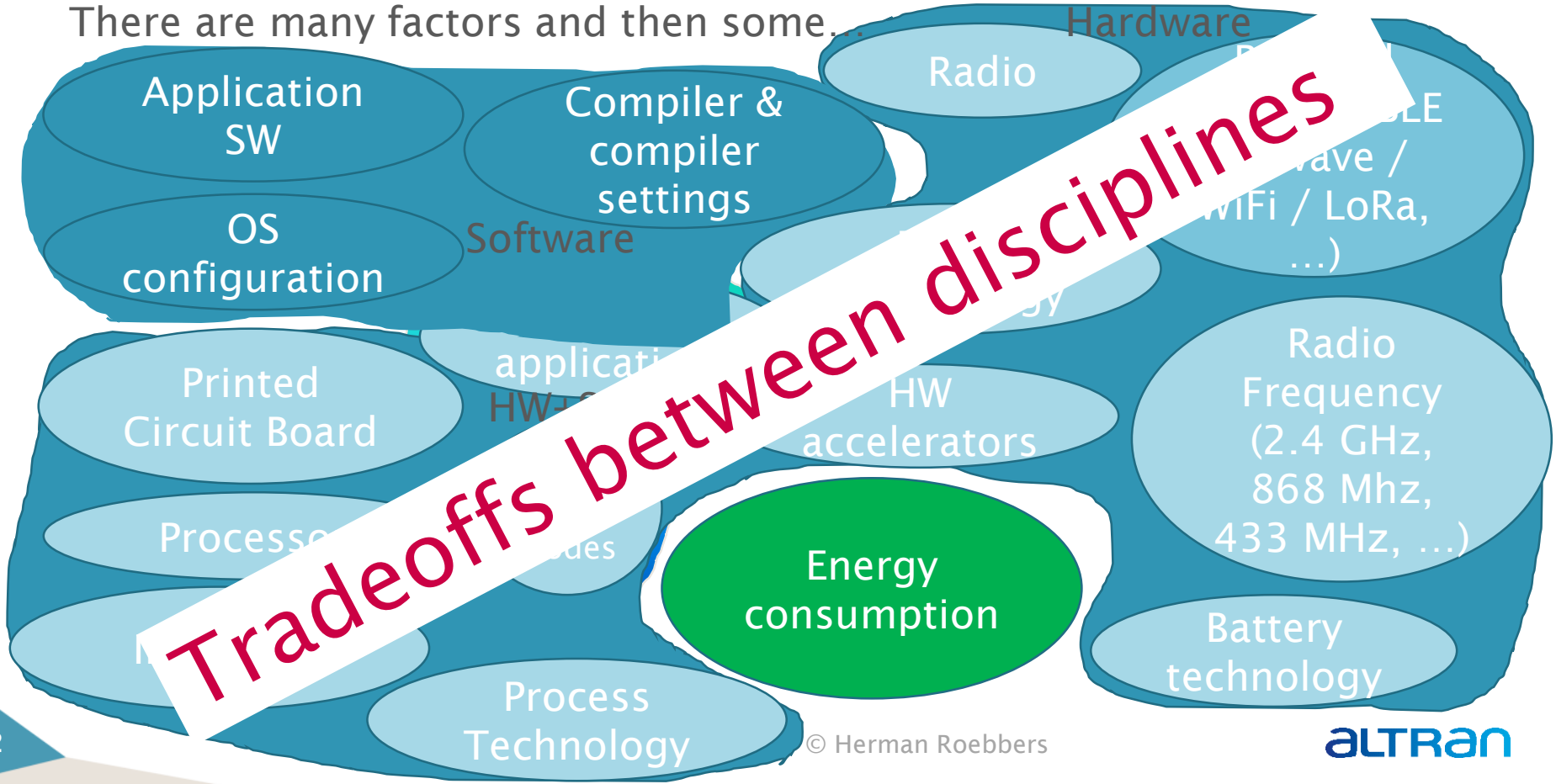

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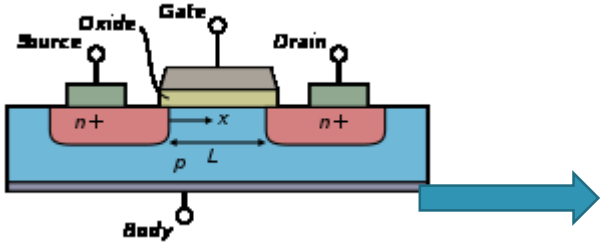
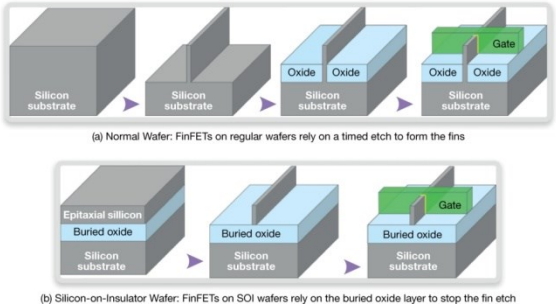
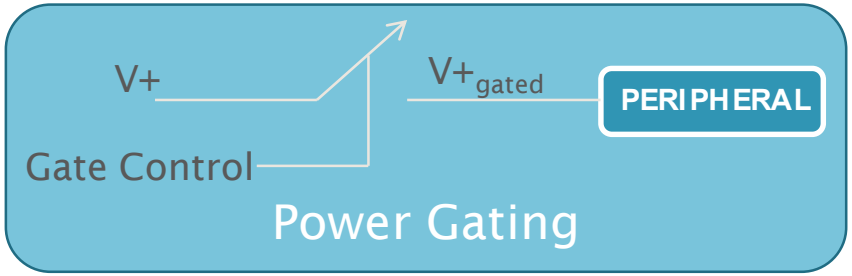
REDUCING ENERGY CONSUMPTION: HARDWARE-ONLY MECHANISMS

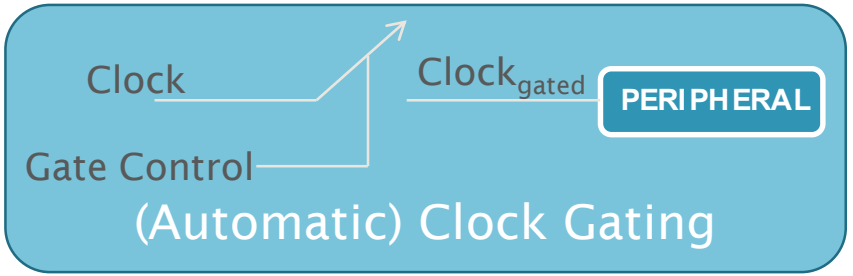
- Board
- Chip
- IP block / chip
- IP block / RTL
- Transistor
- Substrate





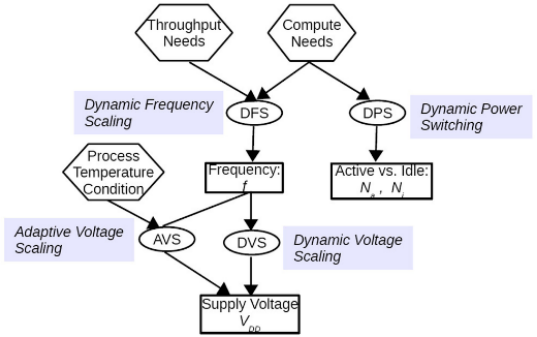
REDUCING ENERGY CONSUMPTION: HARDWARE-ONLY MECHANISMS





Active Mode	110 μA/MHz
Sleep Mode	60 μA/MHz
Mode …	500 nA
Shutoff Mode	20 nA

Energy Modes



Level	Mechanism
Chip	Power gating
	Offer Low Energy modes
	(Automatic) clock gating
	Clock frequency management
	Dynamic Power Switching
	Adaptive Voltage Scaling
	Static Leakage Management
	Hardware Event System/Router

http://www.mdpi.com/jlpea/jlpea-01-00261/article_deploy/html/images/jlpea-01-00261f1-1024.png

REDUCING ENERGY CONSUMPTION: HARDWARE-ONLY MECHANISMS

Level	Mechanism
IP block / chip	Power Gating / State Retention
IP block / RTL	Automatic power / clock gating
Transistor	Select optimum transistor geometry per use case
	FinFET
	TriGate FET
	Sub-threshold operation
	Body Bias
Substrate	Silicon-on-Insulator (SOI)
	Fully Depleted Silicon-on-Insulator (FD-SOI)

REDUCING ENERGY CONSUMPTION: HARDWARE-SOFTWARE MECHANISMS

Level	Mechanism
Board	Dynamic Voltage and Frequency Scaling
	Power Gating via I/O pin
	Controlling Voltage regulator via I/O pin
	Clock Frequency Management
	Controlling device shutdown pins via I/O pin

REDUCING ENERGY CONSUMPTION: SOFTWARE MECHANISMS

Level	Mechanism
Coding	Coding for minimum energy
	Coding for speed
	Cache friendly coding
Operating System	Power API
	Operating point API
	Tickless operation
Driver	Use DMA
	Use HW event mechanism
	Suspend / resume

REDUCING ENERGY CONSUMPTION: SOFTWARE MECHANISMS

The ones you didn't think mattered that much

- Compiler
  - Can make 10's of % difference
- Compiler settings
  - Can make 100's of % difference
- Data and code location

Problem:

- You cannot predict what settings give best results
  - So measure!

REDUCING ENERGY CONSUMPTION: SOFTWARE MECHANISMS

GCC 4.8.3

Routine	Compiler settings	Run-time ms	Code Size	Current mA	Energy uJ
mat_mul_simple	-O2	16.75	192	**2.99**	165.45
mat_mul_faster	-O2	13.00	224	3.06	**129.35**
mat_mul_simple	-O1	17.50	188	3.08	165.45
mat_mul_faster	-O1	15.13	200	3.07	152.14
mat_mul_simple	-O3	16.25	192	3.07	165.13
mat_mul_faster	-O3	15.25	244	3.05	152.52
mat_mul_simple	-Os	25.13	**140**	3.07	253.15
mat_mul_faster	-Os	29.88	168	3.12	307.59**?**
mat_mul_simple	-O0	69.00	264	3.07	**695.20**
mat_mul_faster	-O0	64.75	284	3.11	**661.35**

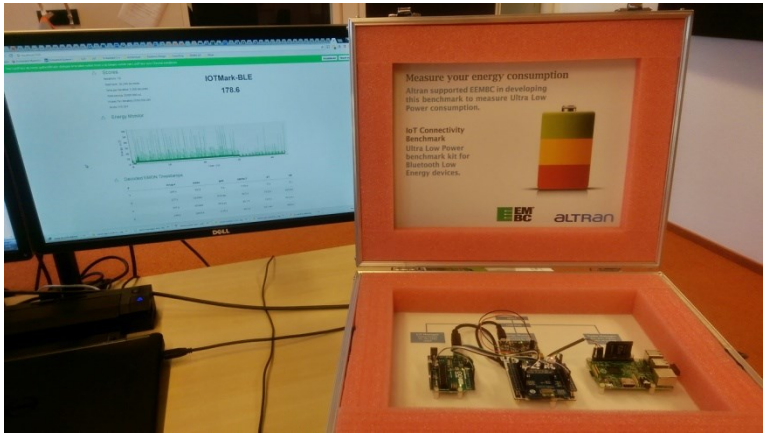
REDUCING ENERGY CONSUMPTION: APPROACH

Software architecture

- From super loop to event driven
- Use DMA to allow CPU to sleep while gathering / sending data
- Use low power modes where possible
- Where possible use hardware mechanisms to have peripherals send each other events without CPU intervention

REDUCING ENERGY CONSUMPTION: APPROACH

When you start, it is good to have a baseline measurement, and compare it to other systems.
The Embedded Microprocessor Benchmarking Consortium (EEMBC, eembc.org) can help with this.



ULP benchmarks*:

- ULPMark
  - -CP (Core Profile, CPU only)
  - -PP (Peripheral Profile, CPU + peripherals)
  - -CM (CoreMark, CPU efficiency)
- IoTMark-BLE
- SecureMark-TLS (Transport Level Security)

*I'm an independent external advisor to these WGs

REDUCING ENERGY CONSUMPTION: APPROACH

If you have a Continuous Integration / Continuous Delivery setup:

- Add energy measurement of operation scenarios to your (smoke) test to notice when a software change results in increased energy consumption.

MCU CHARACTERISTICS FOR ULP:

Characteristic	Typical value
Ultra Low sleep power	20 nA for shutoff, 500 nA (RAM)
Ultra Low Active power	60 μA/MHz from SRAM 100 μA/MHz from flash
Fast, efficient processor	> 1 MIPS/MHz
Very short Wakeup time	2 μs
Effective Low Power Modes	20 nA (shutoff), 500 nA (RAM, CPU retention) 900 nA (RAM, CPU retention, BOD) 45μA/MHz (sleep) 100 μA/MHz (Active)

MCU CHARACTERISTICS FOR ULP (2):

Characteristic	Typical value
Autonomous peripherals	DMA support, operate in sleep
HW event prod./cons. mechanism	Peripheral Reflex System
CPU support for sleep (WFI / WFE)	Cortex-M
Energy efficient peripherals	Low Power/Energy (UART,TIMER)
Energy efficient sensor interface	LESENSE/cap sense
Flash accelerator	
Execution from internal RAM	
FRAM	TI Wolverine, <= 128 KB
Cryptographic HW support	EC, SHA, AES, CRC,
Secure boot, Secure key storage	TrustZone, CryptoCell 310 (Nordic)

FRAM (INSIDE TEXAS INSTRUMENTS MSP430FRX WOLVERINE SERIES)

Non-volatile RAM (FerroElectric RAM)

Advantages:

- Faster than flash (< 50 ns)
- Low voltage (1.5 V), no charge pumps necessary like for flash
  - Less energy
- Byte write, no erase necessary
- (Virtually) unlimited nr of writes (10^{15})
- Programmable division between write-protected and read-write part (Flash based MCU does not give you that option)
- Very resilient against radiation, much better than DRAM or SRAM

Disadvantages

- Lower amount: Currently max FRAM size = 128 kB
- More expensive than flash

CONCLUSIONS

Ultra Low Power is a system thing

- Multiple disciplines (hardware / software)
- Many power reduction mechanisms at different system levels
- Know your hardware
- Hardware/software co-design is best
- For best results
  - Understand available mechanisms
  - Use them wisely

CHALLENGES

Because ULP is a system thing operating on all levels:

- We get a lot more complexity because of relations between levels
- Can we (continue to) abstract from power management?
- How do we keep the power management manageable?

ONLINE ARTICLES

- https://bits-chips.nl/artikel/op-naar-batterijloze-iot-devices/
- https://bits-chips.nl/artikel/hoe-spaar-je-energie-in-een-embedded-systeem/

WANT TO KNOW MORE?

Email me: Herman.Roebbers@Altran.com

Follow my 2-day hands-on workshop:
http://www.hightechinstitute.nl/en/training/software/ultra_low_power_for_internet_of_things/
It is possible to run the workshop on-site

Altran offers various services related to ULP : Power scan, consultancy

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QUESTIONS?