Modeling a hardware platform with POOSL

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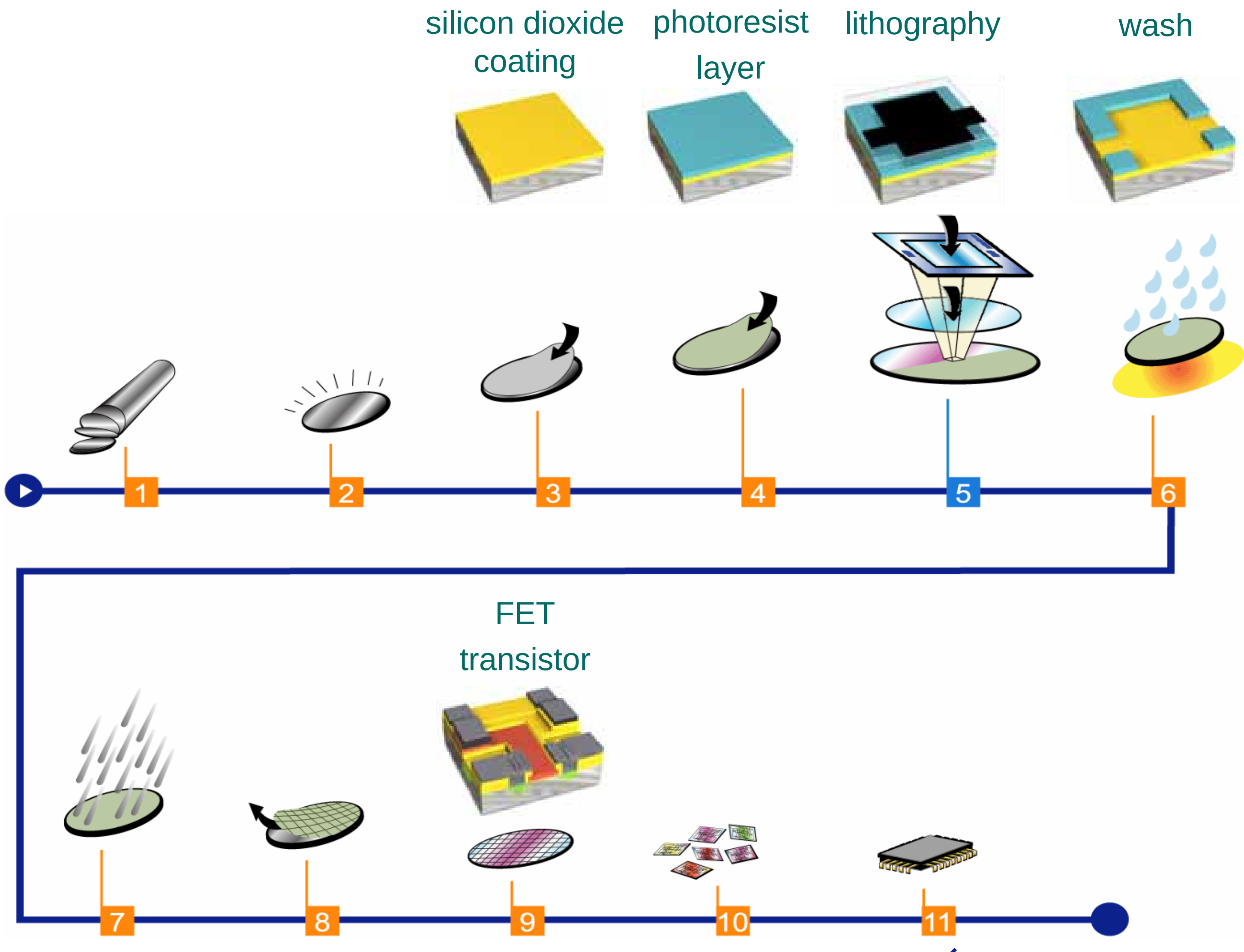
V3

Wafer scanners



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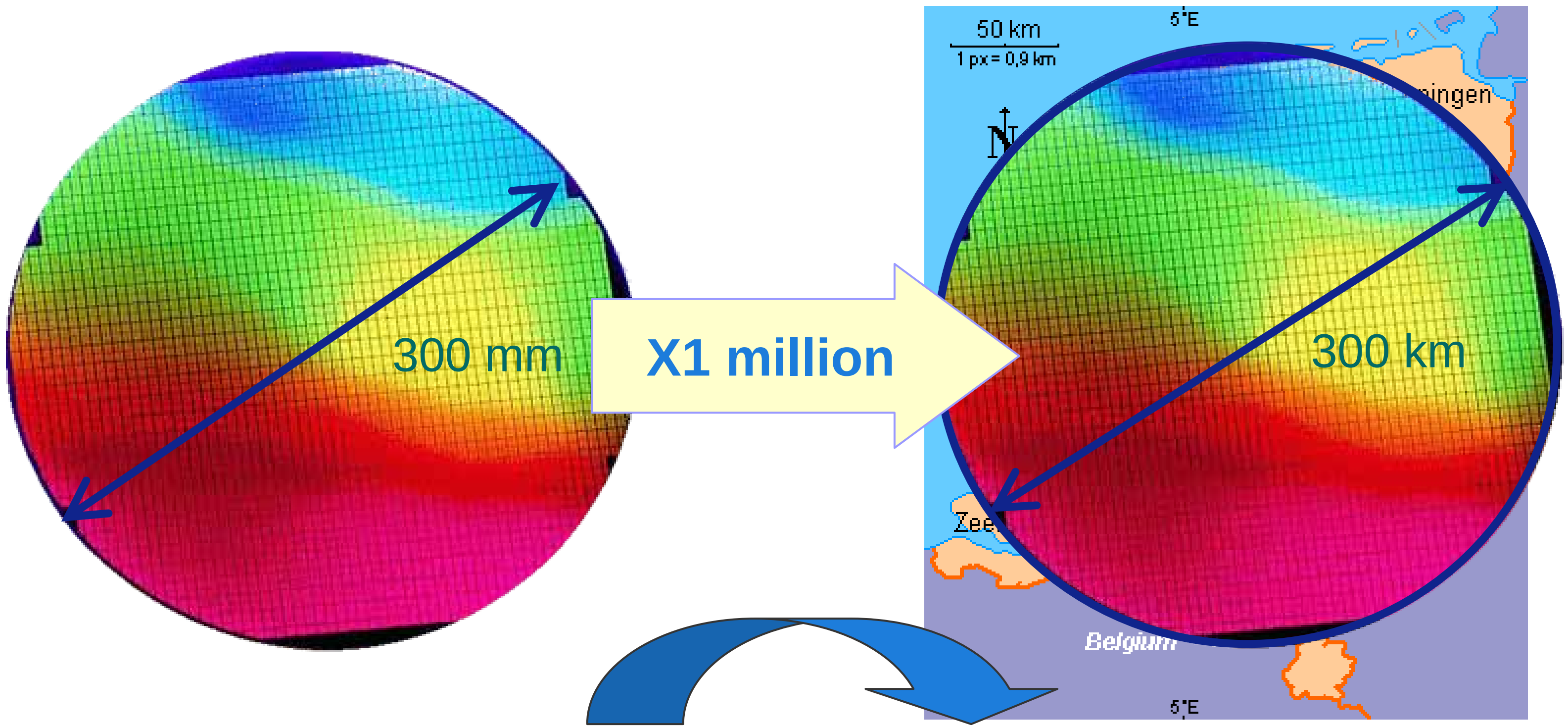
A chip has more than just one layer

Business drivers

Lens		Field Size	Overlay	Throughput
NA	Resolution	X & Y	16-point Alignment	300 mm Wafers 30 mJ/cm2 (125 shots)
Variable 0.85-1.35	≤ 38 nm	26 X 33 mm	≤ 2.5 nm	≥ 175 wph

Print the Netherlands in 30 seconds

300 mm wafer | **The Netherlands**



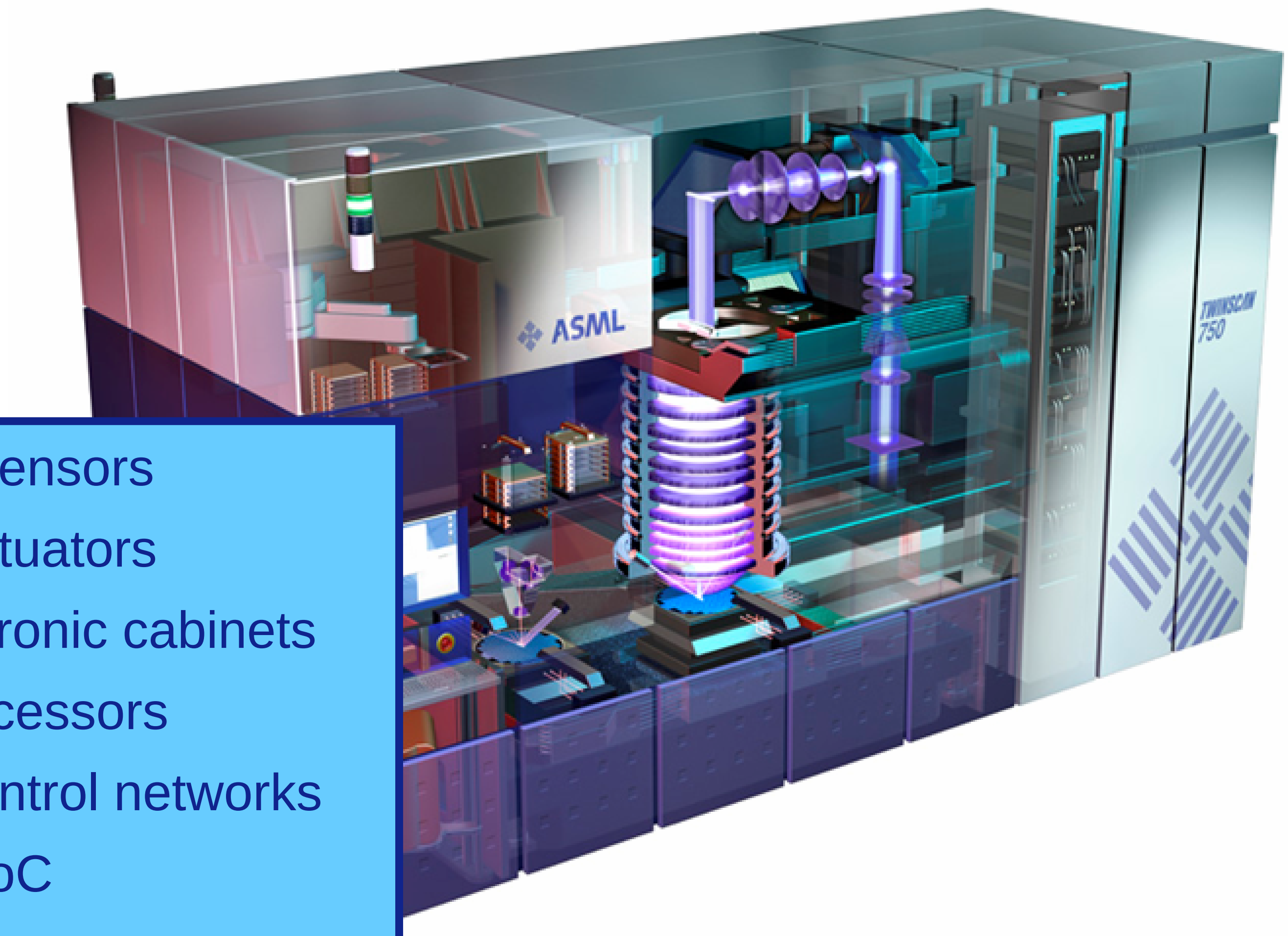
minimum feature size	30 nm
positional accuracy	5 nm

corresponds to	3 cm
positional accuracy	0.5 cm

Photolithography – how an ASML system works

ASML

Embedded control complexity

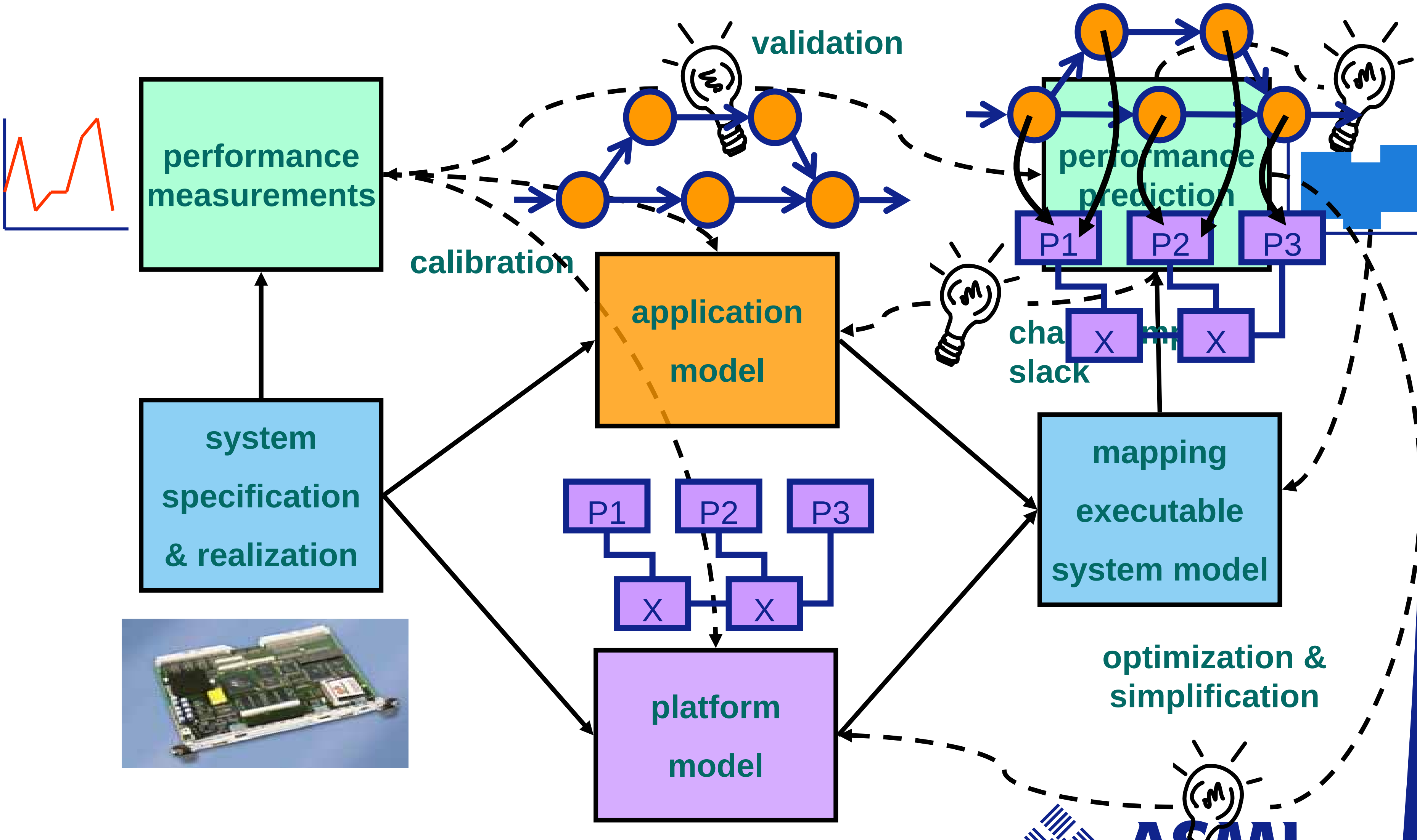


- 1000 sensors
- 500 actuators
- 6 electronic cabinets
- 60 processors
- 200 control networks
- 35 MLoC

Performance modeling and prediction

- Performance modeling knowledge acquired via Wings project
  - Launch on 01-01-2009, duration 1 year
    - Due to the successful results the duration of the project was extended with an additional year
  - Collaboration between ASML and Embedded Systems INSTITUTE
  - Goal is to optimize performance (reduce IO delay) and reduce cost of goods
  - POOSL modeling and Y-Chart approach method used as a vehicle to get detailed insight in system behavior

Approach on performance modeling



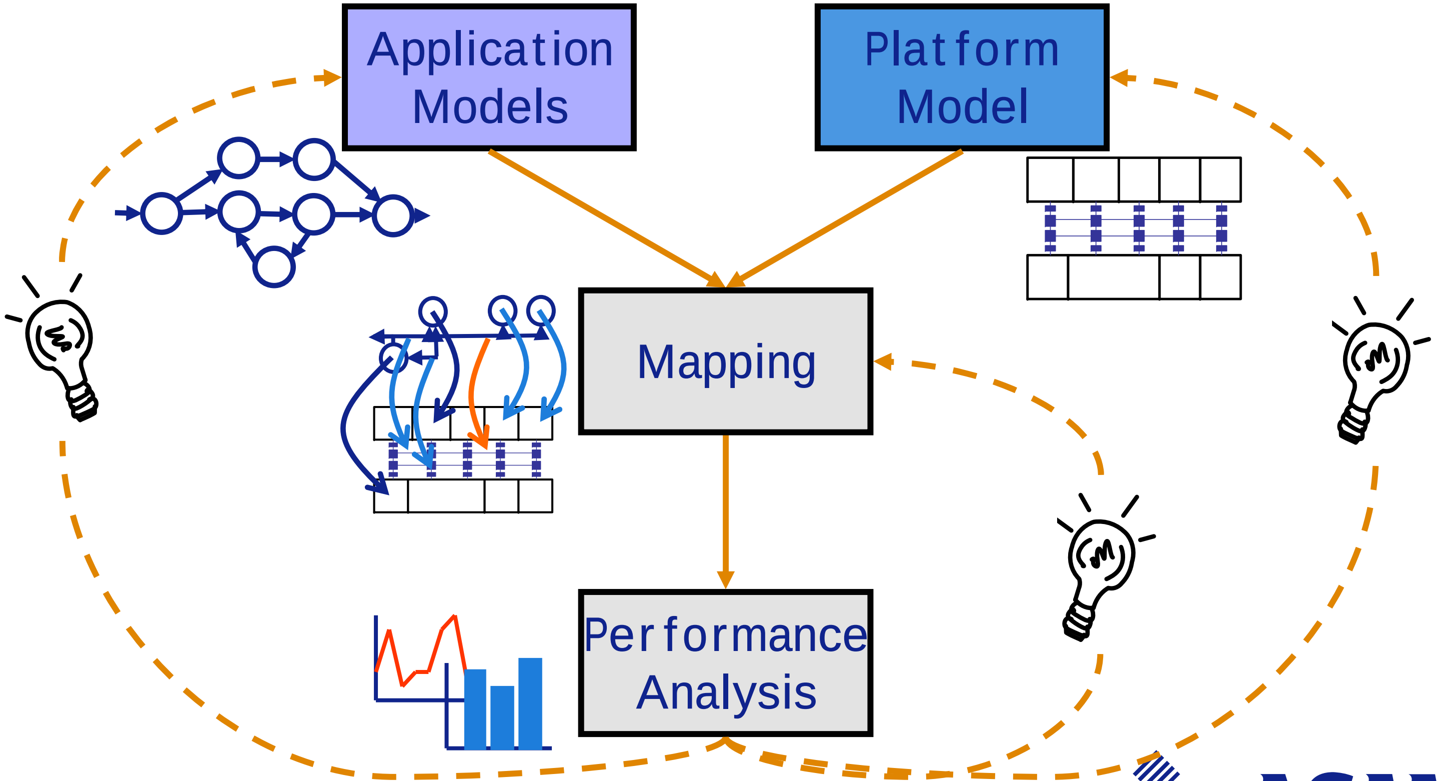
Y-Chart Approach

Design-time performance prediction of

hard & soft real-time dynamic applications

running on

platforms with guaranteed and/or (lossless) best-effort services

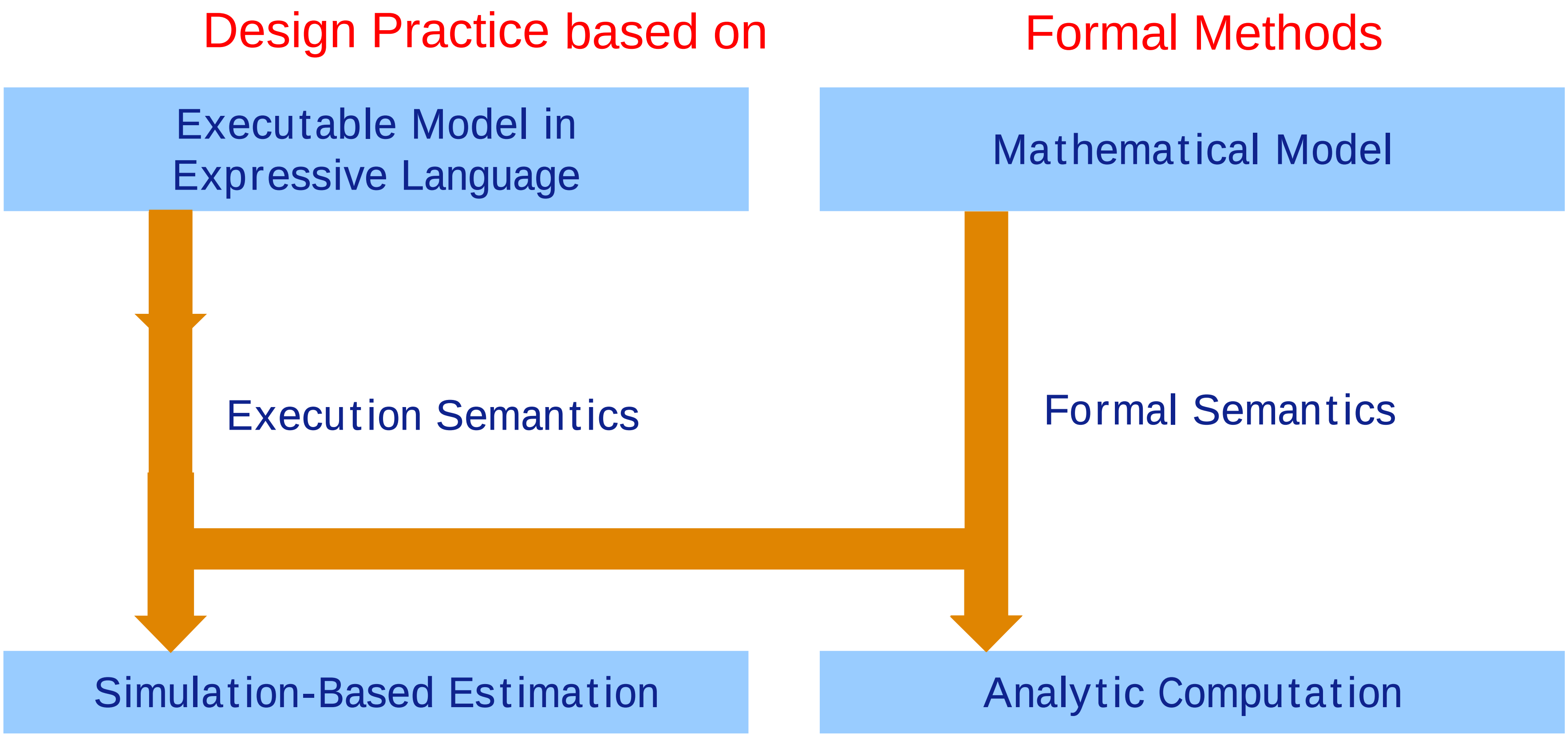


Introduction to POOSL

- Parallel Object-Oriented Specification Language
- Part of SHE Methodology (Software Hardware Engineering)
  - Methodology developed at TU/e

ASML

Performance Analysis with POOSL



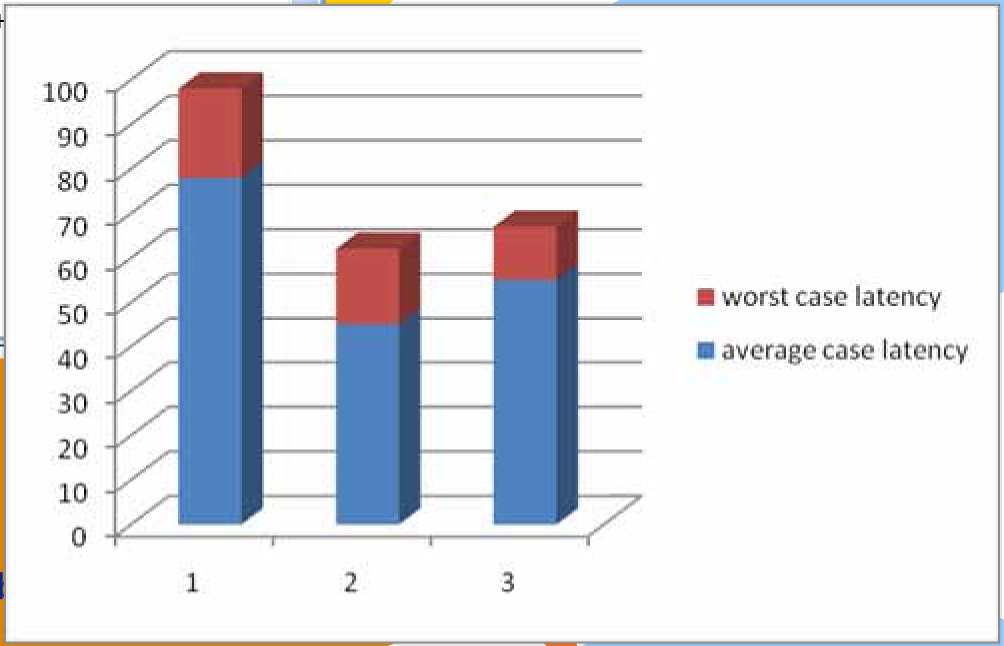
- Modeling convenience
- Estimations with Accuracy
- Scalable
- Tools

- Difficult to make models / Modeling convenience
- Exact results
- Scalability is problematic
- Tools

Formalism: POOSL

Selected Action

```
handleInputPort2()() | p:RIOPacket |
    ip2?packet(p | scheduler inputQueueAccepts(2,p));
    scheduler setOutputPortFor(p);
    par
        if storeAndForwardMode then delay switchLatency +
                                else delay switchLatency
        fi;
        scheduler inputQueuePut(2,p)
    and
        handleInputPort2()()
    rap.
```



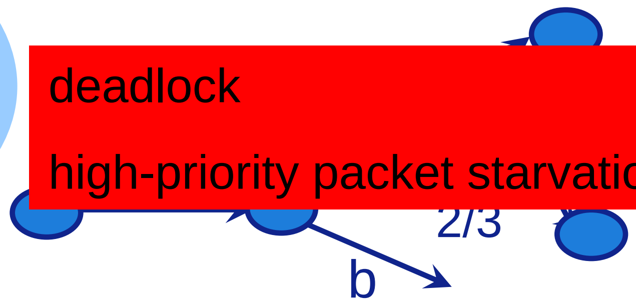
lal

correctness verification

property preserving synthesis

deadlock

high-priority packet starvation



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POOSL design/runtime environments

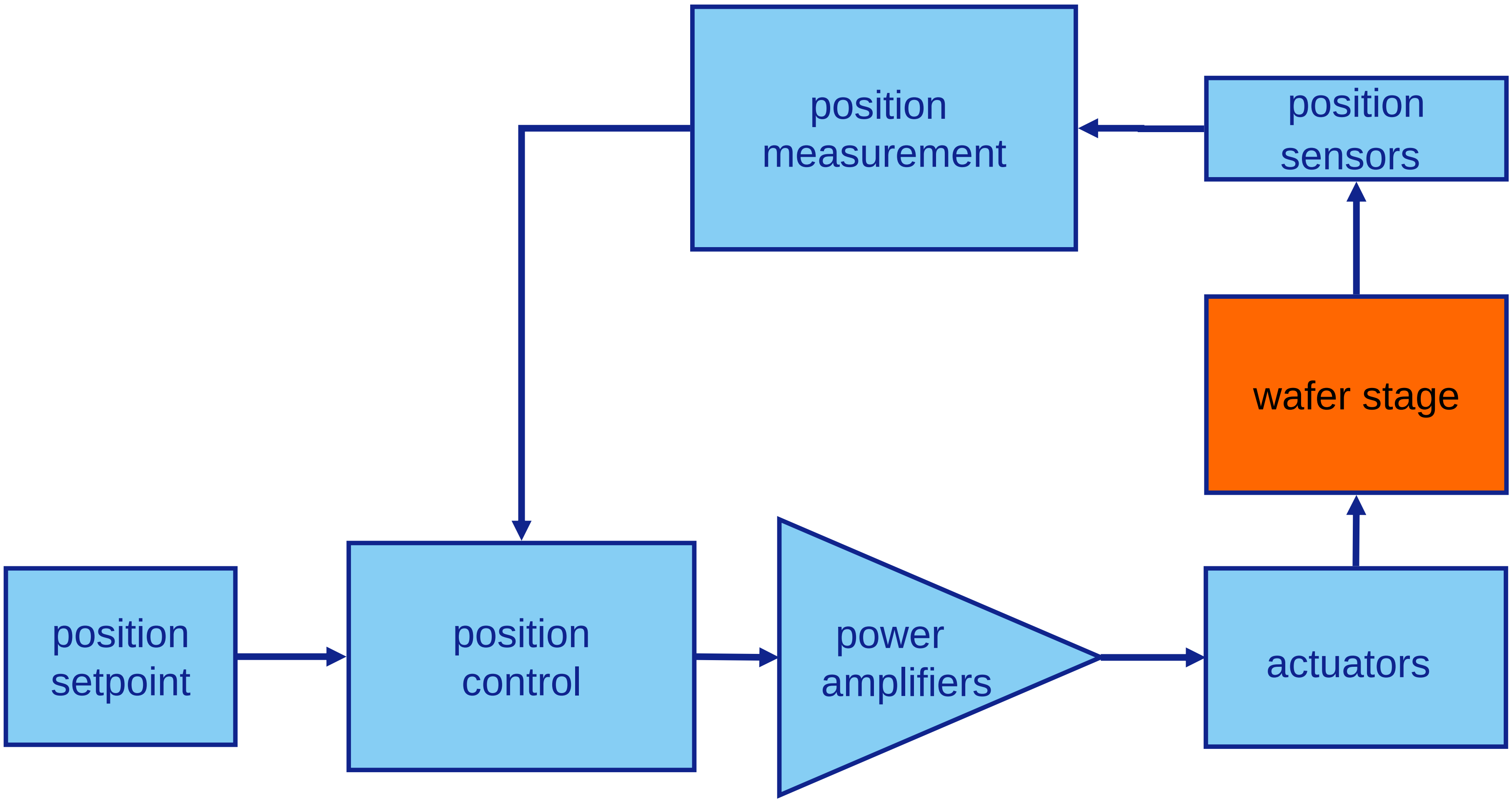
- SHESim
  - A graphical tool for the construction and validation of POOSL models
  - Interprets POOSL semantics runtime
  - Checks during runtime
  - Freeware

- Rotalumis
  - A high-speed execution engine (approx. 100x) for POOSL models
  - Compiles a POOSL model into an intermediate byte code
  - Checks at compile time
  - Freeware

ASML example cases of performance modeling

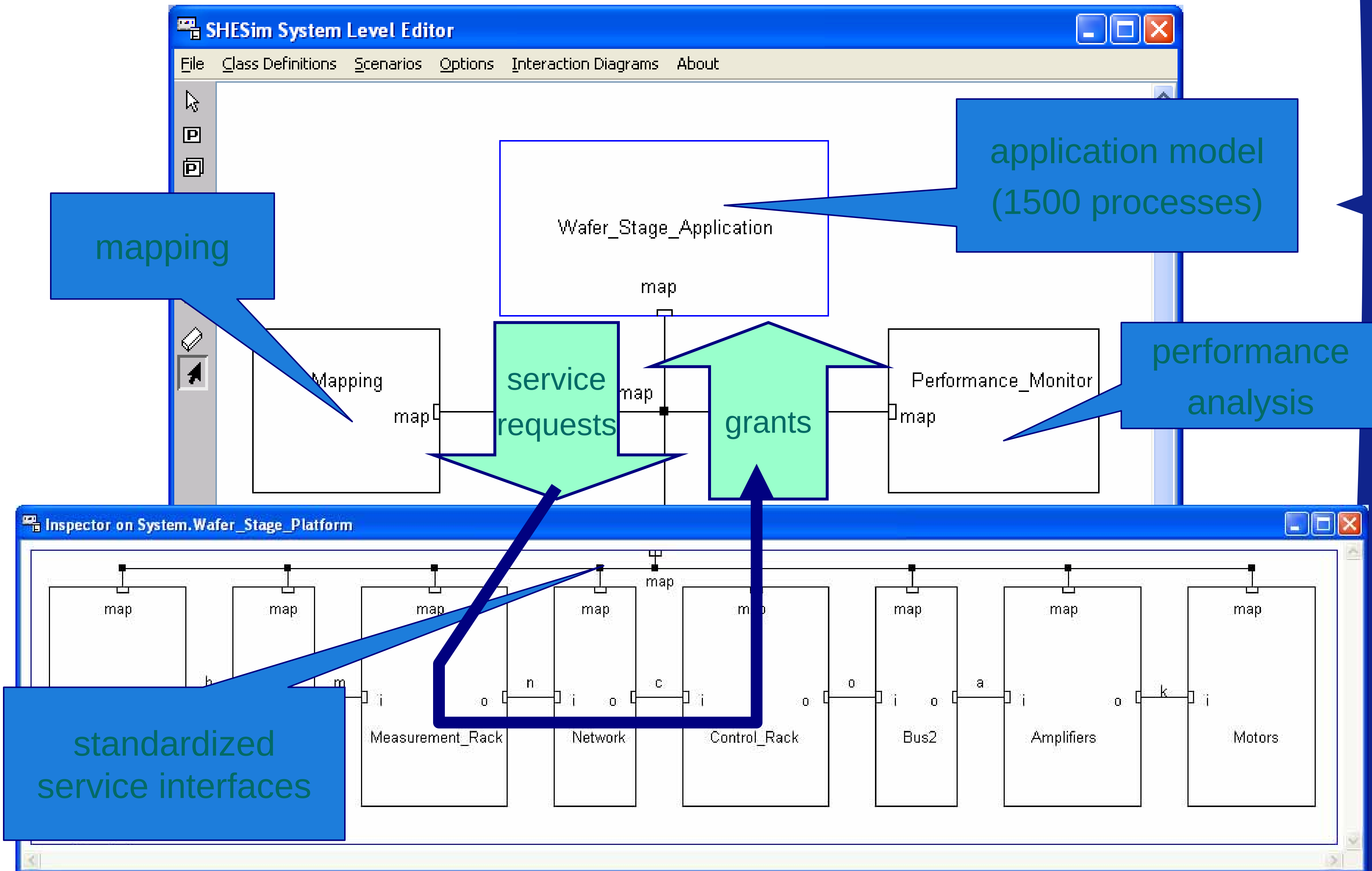
- Case 1: Wafer stage control (Wings)
- Case 2: Performance modeling of a multi-processor system with switched communication networks

Case 1: Wafer stage control (Wings)



hard real-time
period execution

Wafer stage control: executable model



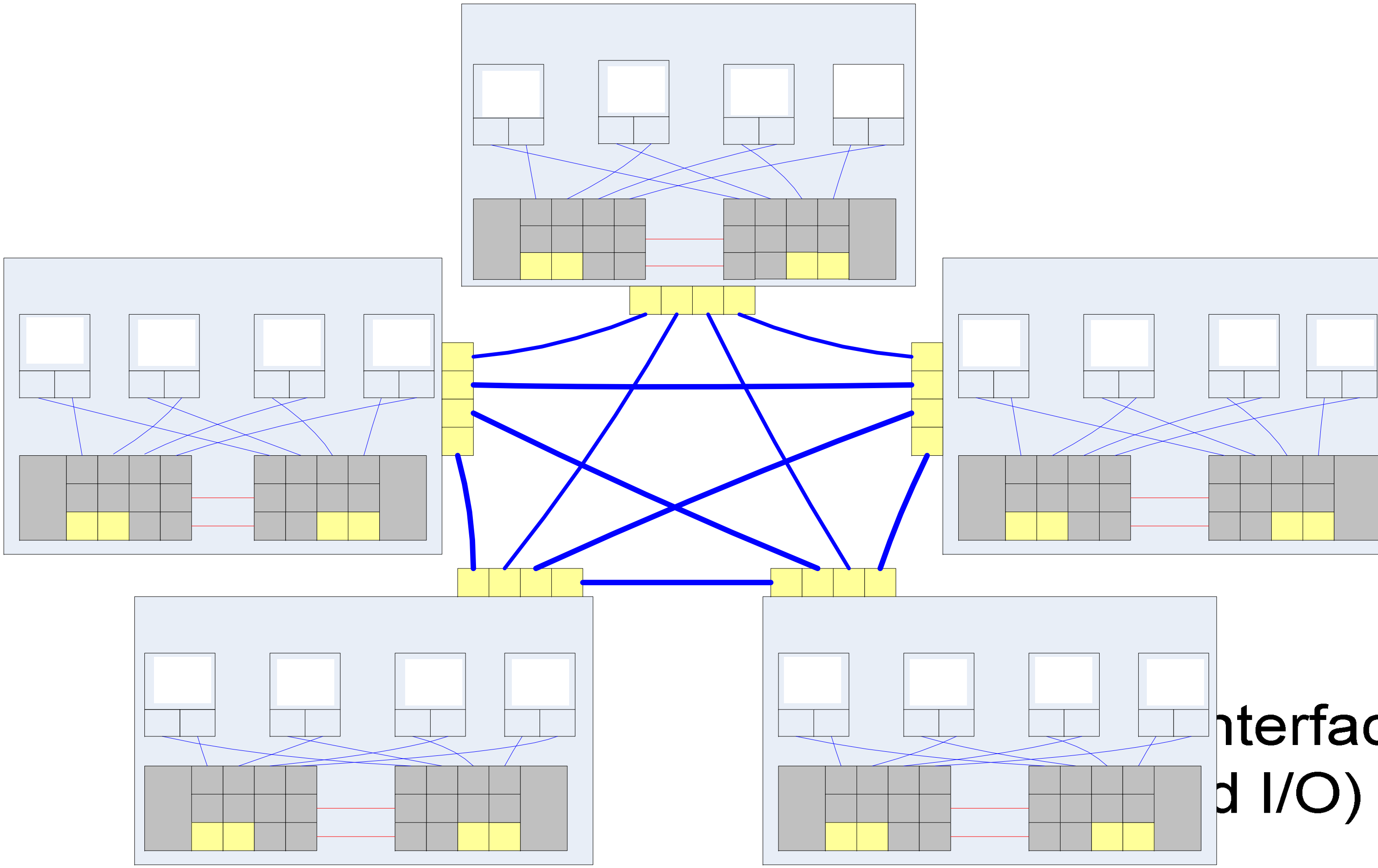
Wings results

- Modeling method to predict and optimize timing performance
- Dissemination
  - workshops
  - ASML is taken up results in various projects
  - embedded software, digital hardware, mechatronics
- Optimizations
  - 16 different improvements identified
  - over 50% performance gain

Case 2: Performance modeling of a multi-processor system with switched communication networks

ASML

Full mesh, SRIO based, switched network topology

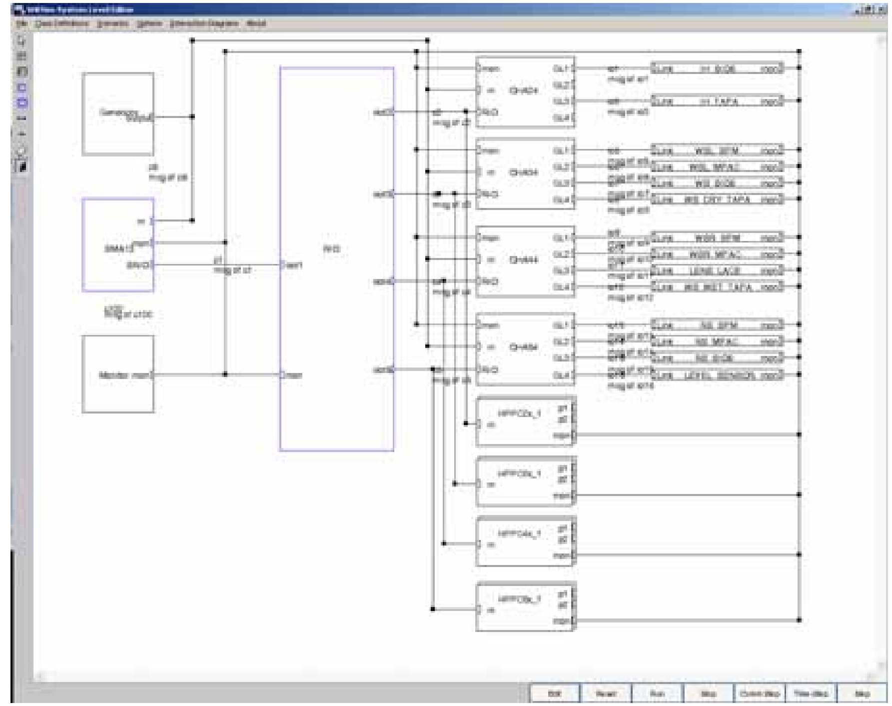


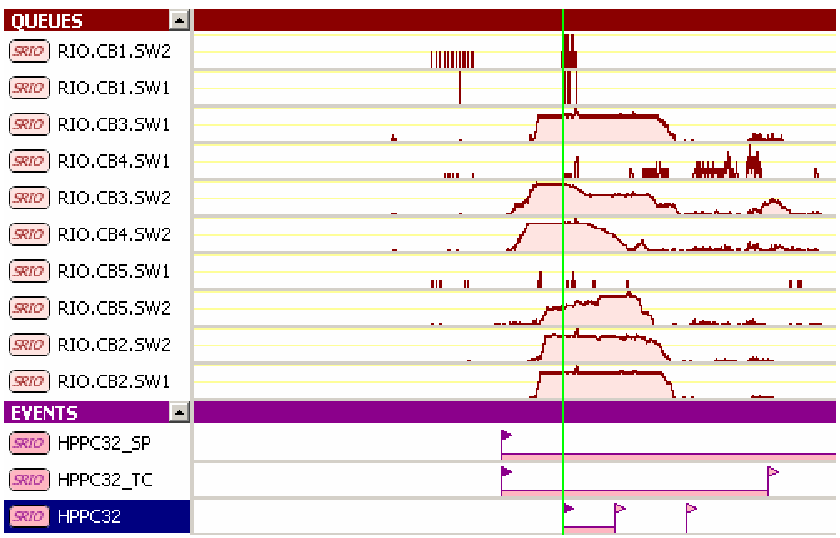
nterface
d I/O)

2.5 Gbps
3.125 Gb

Model and Results

- Reuse of switched network model developed by Wings project.
- Added fully parameterized platform models of motion controllers, IO boards and conductor.
- Application part is described via configuration files.





- Simulation results provided much greater insight in network behavior.
  - For the first time all communication channels are visible at one single moment in time.
  - Unexpected communication delays identified due to heavy traffic on network.

Performance modeling experiences

- Performance modeling has opened the door to a much better understanding of the real-time aspects of an ATCA based motion control system. Some examples:
  - Complex interactions between hardware and software components in a multi-processor environment are easier to analyze.
  - System stability increases due to the fact that complex dependencies which can lead to deadlocks and unforeseen jitter can be detected in advance.
  - Resource usage of hardware and software can be highly optimized.
  - Performance modeling allows complex embedded designs to be verified during design time enabling a smoother integration phase and reduces design risks.
- **Your simulation results are only as good as the knowledge that you put into your model!!!**

ASML